Faculté des Sciences
Unité de recherche CESAM
Laboratoire de Physique des solides, interfaces et nanostructures

Impact of electron trap states on the transport properties of GeSn semiconducting heterostructures assessed by electrical characterizations

Bruno Baert

Dissertation presented in partial
fulfillment of the requirements for the
degree of Doctor in Science

Academic year 2016-2017

Faculté des Sciences
Unité de recherche CESAM
Laboratoire de Physique des solides, interfaces et nanostructures

Impact of electron trap states on the transport properties of GeSn semiconducting heterostructures assessed by electrical characterizations

Jury:

Prof. L. Dreesen (chairman)
Dr. J.-Y. Raty (secretary)
Prof. B. Vanderheyden
Prof. D. Bellet (Université de Grenoble Alpes)
Prof. M. Houssa (Katholieke Universiteit Leuven)
Prof. E. Simoen (Universiteit Gent)
Prof. N.D. Nguyen (promoter)

September 2016

Dissertation presented in partial fulfillment of the requirements for the degree of Doctor in Science

by

Bruno Baert

Academic year 2016-2017

Abstract

The GeSn semiconducting alloy possesses many attractive properties, such as a direct bandgap and increased carrier mobilities. It is, among other potential applications, expected to be used in next generation complementary Metal-Oxide-Semiconductor (MOS) devices with boosted performances. Because of the lattice mismatch with Ge or Si, it can be used as a stressor or or strained material. It is therefore also a good candidate as compressive stressor for the source and the drain in p-type Ge-channel MOS field-effect transistors or as channel material itself. Although the growth of GeSn materials with high crystalline quality has been achieved in the recent years, a complete and accurate characterization of defects as well as an assessment of their influence in such materials has not been performed yet.

This thesis is dedicated to the study of the impact of electronic trap states in GeSn semiconducting heterostructures. The electrical transport properties of both pn junction diodes and MOS structures were investigated using a variety of experimental techniques. Detailed theoretical analysis with a numerical simulation tool designed on purpose was also performed, both to enable the interpretation of experimental measurements and to evaluate the use of routine characterization techniques such as the conductance method when applied specifically to low bandgap materials like GeSn.

The electrical characteristics of p-GeSn/n-Ge diodes grown by chemical vapor deposition with 5.8% Sn were analyzed and the presence of traps was assessed. The combined approach, harnessing simultaneously experimental measurements and numerical simulations, allowed to determine the critical properties of the traps that were revealed at the GeSn/Ge interface. In a second step, the transient currents resulting from the lack of passivation of mesa diodes were explored and modeled appropriately by different approaches.

Concerning the assessment of the impact of traps in GeSn MOS structures, we studied and discussed their effect on the typical features found in capacitance-voltage characteristics. The applicability of the conductance

method was also shown to be strongly dependent on the inversion response of minority carriers and we demonstrated the extraction of the interface trap density using this technique for various trap energy levels and concentrations. The relationship between the applied bias and the Fermi level at the interface, as well as the link with the interface trap time constants and capture cross sections were detailed and consequently explained. The dependence of the onset of the inversion response was then further examined, where it was concluded that the bandgap energy value dramatically alters the strength of the inversion response. The influence of the minority carrier mobility and effective mass was ultimately elucidated, which enabled to support the physical interpretation of the measurements performed on fabricated MOS structures.

Résumé

L'alliage semi-conducteur GeSn possède de nombreuses propriétés très attrayantes, telles qu'une bande d'énergie directe et des mobilités de porteurs de charge accrues. Son utilisation, entre autres applications potentielles, dans les dispositifs CMOS (Complementary Metal-Oxide-Semiconductor) de prochaine génération est attendue avec des performances améliorées. En raison du désaccord de maille avec le germanium et le silicium, il peut être utilisé en tant que matériau générant de la contrainte ou subissant de la contrainte mécanique. Il est dès lors un bon candidat à l'intégration dans des transistors MOS à effet de champ à canal de Ge, induisant des contraintes en compression sur la source et le drain, ou dans des dispositifs où il forme le matériau de canal lui-même. Bien que la croissance de GeSn de haute qualité cristalline ait été réalisée dans les années récentes, une caractérisation complète et précise des défauts, ainsi qu'une évaluation de leur influence dans ce matériau, n'ont pas encore été obtenues à ce jour.

Cette thèse est dédiée à l'étude de l'impact des états électroniques de piège au sein d'hétérostructures semi-conductrices à base de GeSn. Les propriétés électriques de diodes à jonction pn ainsi que de structures MOS ont été examinées à l'aide de techniques expérimentales. Une analyse théorique détaillée a été réalisée grâce à un outil de simulation numérique spécialement mis au point pour à la fois permettre l'interprétation des mesures expérimentales et évaluer l'utilisation de techniques de caractérisation de routine, telles que la méthode de la conductance, lorsqu'elles sont appliquées spécifiquement à des matériaux à faible bande interdite comme le GeSn.

Les caractéristiques électriques de diodes p-GeSn/n-Ge fabriquées par déposition sous vapeur chimique avec 5.8% d'étain ont été analysées et la présence de pièges a été testée. L'approche combinée, exploitant simultanément les mesures expérimentales et les simulations numériques, a permis de déterminer les propriétés critiques de pièges qui ont été révélés à l'interface GeSn/Ge. Dans une deuxième étape, les courants transitoires résultant du

défaut de passivation de diodes mesa ont été explorés et modélisés de manière appropriée par différentes approches.

En ce qui concerne l'évaluation de l'impact des pièges dans les structures MOS à base de GeSn, nous avons étudié et discuté les effets de ceux-ci sur les traits typiques des caractéristiques capacité-tension. Nous avons également mis en évidence que la pertinence de la méthode de la conductance est fortement dépendante de la réponse en inversion des porteurs minoritaires et nous avons démontré l'extraction de la densité d'états de piège d'interface en utilisant cette technique pour divers niveaux d'énergie et de concentration de pièges. La relation entre la tension appliquée et le niveau de Fermi à l'interface, ainsi que le lien entre les constantes de temps des pièges d'interface et les sections de capture, ont été détaillés et expliqués en conséquence. La dépendance du seuil de la réponse en inversion a alors été examinée plus en profondeur et nous avons conclu que la largeur de la bande interdite altère de manière dramatique l'amplitude de la réponse en inversion. Finalement, l'influence de la mobilité des porteurs minoritaires et de la masse effective a été élucidée, ce qui a permis de corroborer l'interprétation physique des mesures réalisées sur les structures MOS fabriquées.

Acknowledgements

I would first like to thank my advisor, Prof. Ngoc Duy Nguyen, for giving me the opportunity to perform this journey in the world of solid-state physics and research. I am grateful for the support, advice and encouragement he offered me during all this time.

I am very thankful, too, for the collaboration developped with all the people I came in contact with in IMEC. I am especially indebted to the useful advices of Prof. Eddy Simoen, Dr. Roger Loo and the work of Somya Gupta, Dr. Yosuke Shimura and Dr. Federica Gencarelli.

The technical help of Xavier Baumans and Emile Fourneau was also of paramount importance to the realization of this work, be it for the wire-bonding of samples or the metal contacts evaporation.

I would like to thank Dr. Jean-Yves Raty and Prof. Benoît Vanderheyden for serving on my committee and following my progress over these years.

Prof. Laurent Dreesen, Prof. Daniel Bellet and Prof. Michel Houssa are warmly thanked for accepting to serve on my jury and evaluate this thesis.

Special thanks go to Dorian Baguette, for his friendship and fruitful discussions on many aspects of my work.

I could not have reached this stage, either, without the permanent support and encouragements of my parents, brother, sister, grandparents and friends. Their unconditional faith in my success was, especially at times, of incredible value.

Finally, though she certainly ought to have been mentioned first, I would like to bless an extraordinary person, Fanny, for enduring me and continuously supporting me. I am utterly grateful for your love.

Contents

List of Acronyms **xi**

List of Symbols **xiii**

1 Introduction **1**

2 GeSn, a group-IV semiconducting alloy **7**
2.1 Motivations 7
2.2 Growth methods 8
2.2.1 $Ge_{1-x}Sn_x$ crystalline structure and growth challenges . 8
2.2.2 Molecular Beam Epitaxy 10
2.2.3 Chemical Vapor Deposition 11
2.3 $Ge_{1-x}Sn_x$ energy band structure and electronic properties . . 13
2.3.1 Direct bandgap 13
2.3.2 Carrier mobility boost in Ge 15
2.4 $Ge_{1-x}Sn_x$ applications 17
2.4.1 High mobility CMOS devices 17
2.4.2 Optoelectronic applications 19

3 Electrical characterization methods **21**
3.1 Introduction 22
3.2 Schottky diodes and pn junctions 23
3.2.1 I-V characterization 23
3.2.2 C-V characterization 25
3.3 Principles of impedance spectroscopy 27
3.3.1 Impedance and complex formalism 27
3.3.2 Impedance, admittance and the complex plane 28
3.3.3 Equivalent electrical circuit modeling 30
3.3.4 Representation of admittance data 32
3.4 MOS structures 34

3.4.1 Ideal admittance behaviour of a MOS capacitor 34
3.4.2 The conductance method 37
3.5 Experimental setup 43
3.5.1 Temperature-dependent measurements 44
3.5.2 Sample holder 45

4 Numerical simulations 47
4.1 The basic semiconductor equations 47
4.1.1 Poisson's equation 47
4.1.2 Continuity equations 49
4.1.3 Transport equations 53
4.2 Numerical resolution 58
4.2.1 Dependent variables and physical parameters 59
4.2.2 Meshing, scaling and discretization 59
4.2.3 Boundary conditions 66
4.2.4 Linearization and solving algorithms 67

5 GeSn based pn junctions 73
5.1 Theoretical investigation and simulations 76
5.2 Samples 80
5.3 Electrical characterization 81
5.3.1 Current-voltage characteristics 81
5.3.2 Capacitance-voltage characteristics 89
5.4 Effect of passivation on current transients in reverse-biased diodes 94
5.5 Conclusions 108

6 GeSn based MOS structures 111
6.1 Simulation of interface traps in MOS structures 114
6.2 Capacitance-Voltage characteristics 115
6.2.1 Interface trap density and energy position 120
6.2.2 Effect of temperature 123
6.3 The conductance method 125
6.3.1 Discrete energy levels 128
6.3.2 Extended energy distributions 133
6.3.3 Interface traps time constant 138
6.4 Inversion response of minority carriers 140
6.4.1 High-k gate stacks 142
6.5 Equivalent circuit analysis of GeSn capped MOS structures . 146
6.5.1 Samples 146

6.5.2 Impedance data and electrical model 148
6.6 Conclusions 151

7 Conclusions **153**
7.1 Achievements 154
7.1.1 GeSn/Ge pn diodes 154
7.1.2 GeSn MOS devices 156
7.2 Perspectives 158

A Equivalent electrical model **161**
A.1 Parallel RC and RC series circuits 161
A.2 Parallel RC circuit with a series resistance 162
A.3 Two parallel RC circuits in series 163
A.4 Two parallel RC circuits and a series resistance 164

B Linearization of the discretized equations **165**
B.1 Poisson's equation 165
B.2 Electron continuity equation 166
B.3 Hole continuity equation 168
B.4 Trap level occupancy continuity equation 170

C Optoelectrical characterization of pGeSn/n$^+$Ge/nGe layers **173**
C.1 pGeSn/n$^+$Ge/nGe layers 173
C.2 Absorption 175
C.3 Metal contact deposition 176

D $GeSnO_2$ and GeO_2 MOS capacitors **179**

Bibliography **184**

Publications and communications **207**

List of Acronyms

Acronym	Signification
AES	Auger Electron Spectroscopy
ARXPS	Angle Resolved X-ray Photoelectron Spectroscopy
BTBT	Band to Band Tunneling
BTE	Boltzmann Transport Equation
C-V	Capacitance-Voltage
CMOS	Complementary Metal Oxide Semiconductor
CPU	Central Processing Unit
CVD	Chemical Vapor Deposition
DLTS	Deep Level Transient Spectroscopy
EOT	Equivalent Oxide Thickness
ESR	Electron Spin Resonance
FDM	Finite-Difference Method
FEM	Finite Elements Method
I-V	Current-Voltage
IEEE	Institute of Electrical and Electronics Engineers
IL	Interfacial Layer
IR	Infrared
IRDS	International Roadmap for Devices and Systems
ITRS	International Technology Roadmap for Semiconductors

Acronym	Signification
MBE	Molecular Beam Epitaxy
MOS	Metal Oxide Semiconductor
MOSFET	Metal Oxide Semiconductor Field-Effect Transistor
PCB	Printed Circuit Board
RHEED	Reflection High Energy Electron Diffraction
RIE	Reactive-Ion Etching
RSM	Reciprocal Space Mapping
RT	Room Temperature
S/D	Source-Drain
SIMS	Secondary Ion Mass Spectroscopy
SRB	Strain Relaxed Buffer
SRH	Shockley-Read-Hall
TAT	Trap Assisted Tunneling
TEM	Transmission Electron Microscopy
UHV	Ultra High Vacuum
XPS	X-ray Photoelectron Spectroscopy
VS	Virtual Substrate
XRD	X-Ray Diffraction

List of Symbols

Symbol	Unit	Description
A	m^2	Surface area
A^*	$Am^{-2}K^{-2}$	Effective Richardson constant
a_0	Å	Relaxed lattice constant
B	T	Magnetic field
B	S	Susceptance
B_r	m^3s^{-1}	Radiative recombination constant
C	F	Capacitance
C_{ox}	F	Oxide capacitance
C_s	F	Semiconductor capacitance
D	Cm^{-2}	Electric displacement field
D_{it}	cm^{-2}	Interface trap density
D_n	m^2s^{-1}	Diffusion coefficient of electrons
D_p	m^2s^{-1}	Diffusion coefficient of holes
E	V/m	Electric field
e_{ct}	$m^{-3}s^{-1}$	Rate of emission from the trap level to the conduction band
E_F	eV	Fermi level
E_g	eV	Bandgap energy
ϵ_0	Fm^{-1}	Vacuum permittivity
ϵ_r	-	Semiconductor dielectric constant

Symbol	Unit	Description
e_{vt}	$m^{-3}s^{-1}$	Rate of emission from the trap level to the valence band
f_{it}	Hz	Peak frequency of interface traps
F_n	eV	Electron quasi-Fermi level
F_p	eV	Hole quasi-Fermi level
F_t	eV	Traps quasi-Fermi level
G	S	Conductance
g_n	$m^{-3}s^{-1}$	Optical electron generation rate
G_P	S	Equivalent parallel conductance
g_p	$m^{-3}s^{-1}$	Optical holes generation rate
g_t	-	Degeneracy factor of the traps
$(G_P/\omega)_{\max}$	S s	Maximum value of G_p/ω as a function of frequency
$\mathbf{H}$	A m^{-1}	Magnetic field
h	m^2kg s^{-1}	Planck constant
HF	-	Hydrofluoric acid
H_2O_2	-	Hydrogen peroxide
I_0	A	Reverse saturation current
$\mathbf{J}$	A/m^2	Current density
k	JK^{-1}	Boltzmann constant
L_n	m	Diffusion length of electrons
L_p	m	Diffusion length of holes
μ_n	cm^2/Vs	Electron mobility
μ_p	cm^2/Vs	Hole mobility
m_e	kg	Electron mass
m_e^*	kg	Electron effective mass
m_p^*	kg	Hole effective mass
m_T^*	kg	Transverse electron effective mass
m_L^*	kg	Longitudinal electron effective mass

Symbol	Unit	Description
m^*_{HH}	kg	Heavy hole effective mass
m^*_{LH}	kg	Light hole effective mass
n	-	Ideality factor
n	cm^{-3}	Electron concentration
N_A	cm^{-3}	Acceptor dopant concentration
N_c	cm^{-3}	Effective density of states in the conduction band
N_D	cm^{-3}	Donor dopant concentration
N_{eff}	cm^{-3}	Effective density of states of the majority carrier band
n_i	cm^{-3}	Intrinsic carrier concentration
N_t	cm^{-3}	Total trap concentration
n^*_t	cm^{-3}	Negative charge resulting from the trap concentration N_t
N_v	cm^{-3}	Effective density of states in the valence band
Φ	$m^{-2}s^{-1}$	Flux of incident photons
ϕ_s	V	Surface potential
ϕ_b	eV	Schottky barrier height
ψ	V	Electric potential
p	cm^{-3}	Holes concentration
q	C	Electron charge
ρ	C/m^3	Electric charge density
R	Ω	Resistance
R_s	Ω	Series resistance
R_n	$m^{-3}s^{-1}$	Recombination term for the electrons
R_p	$m^{-3}s^{-1}$	Recombination term for the holes
r_{ct}	$m^{-3}s^{-1}$	Rate of recombination from the conduction band to the trap level
r_{bb}	$m^{-3}s^{-1}$	Rate of band-to-band recombination

Symbol	Unit	Description
r_{vt}	$m^{-3}s^{-1}$	Rate of recombination from the valence band to the trap level
σ_n	m^2	Electron capture cross section
σ_p	m^2	Hole capture cross section
σ_p^o	m^2	Hole optical capture cross section
σ_n^o	m^2	Electron optical capture cross section
SF_6	-	Sulfur hexafluoride
SiO_2	-	Silicon oxide
T	K	Temperature
t	nm	Thickness
t_{ox}	m	Oxide thickness
τ_n	s	Electron relaxation time
τ_p	s	Holes relaxation time
V_d	V	Built-in potential
V_{fb}	V	Flatband potential
v_n^{th}	m/s	Thermal velocity of electrons
v_p^{th}	m/s	Thermal velocity of holes
W_d	m	Depletion width
ω	rad s^{-1}	Angular frequency
X	Ω	Reactance
Y	S	Admittance
Z	Ω	Impedance

Chapter 1

Introduction

$Ge_{1-x}Sn_x$ has been known to show semiconducting properties since 1960 [1]. It initially did not attract strong interest, though, because of the substantial difficulties involved in the growth of materials with a significant Sn content ($> 1\%$) and sufficient crystalline quality [2, 3]. The quest for new semiconductor materials with improved properties and the recent progress in the growth of $Ge_{1-x}Sn_x$ [4] has renewed interest for this alloy developed since around 2007.

Alloying Sn with Ge results in a new material with characteristics that are widely different from those of either Ge or Sn. The band structure of Ge is considerably altered by the introduction of the much larger Sn atoms, and the bandgap energy is reduced. A direct bandgap material is even obtained for a Sn content over approximately 9% [4]. The larger lattice constant of GeSn as compared with other group-IV semiconductors such as Si or Ge allows to induce compressive or tensile strains, and subsequently improve the charge carrier mobilities in those materials via effective mass engineering. These two main properties have led GeSn[1] materials to be considered as an interesting candidate material for next generation high performance transistors and for long wavelength optoelectronic applications that can be directly integrated with the existing Si platform.

Silicon has been in the heart of semiconductor technology for the last 50 years. This historical prominence is directly linked to the low cost of producing Si, as compared to other materials such as Ge, to its strong mechanical properties due to the crystallization in the diamond form, and its very stable associated oxide SiO_2. This historically enabled the design and man-

[1] GeSn and $Ge_{1-x}Sn_x$ will be used with an equivalent signification throughout this work, unless otherwise mentioned.

ufacturing of metal-oxide-semiconductor field-effect transistors (MOSFETs) with increasingly high performances. Since the discovery of the transistor by Bardeen, Brattain and Shockley in 1947, the physical dimensions of Si MOSFETs have steadily shrunk down to allow an increased integration of elementary devices into electronics chips, a process defined as *downscaling* [5]. The famous, self-fulfilling prophecy known as Moore's law, even stated in 1965 that the integration of devices would double every two years [6]. This trend was more or less abided by until recently, with characteristic features of MOSFETs scaling from 10 µm in 1971 down to 14 nm in 2014 [7], a dramatic reduction of almost 3 orders of magnitude.

Recently, though, reducing the physical size of transistors did not bring significant performance improvements anymore [8]. When the transistor channel length approached 100 nm, 10 years ago, further reducing the dimensions also started to introduce serious additional challenges for their fabrication [9], raising the cost of further technological development. In addition, at this extreme size reduction stage, the on-state current of MOSFETs decreases whereas the off-state current increases, which brings in another drawback because of the overall decrease in the current driving capability and the relative increase of power consumption of complementary metal-oxide-semiconductor (CMOS) transistors, which are themselves based on MOSFETs.

As a further indication of the looming dead end of this approach, the International Technology Roadmap for Semiconductors (ITRS), which has been setting the direction for semiconductor technology developments since 1993, has announced that its final roadmap would be issued in 2016. New initiatives exploring wider fields for performance development are now explored by ITRS 2.0 [10, 11] as well as the subsequent International Roadmap for Devices and Systems (IRDS) [12] in collaboration with the Institute of Electrical and Electronics Engineers (IEEE).

The further development of the performance of MOSFETs does not rely solely upon shrinking the size of the devices, anymore. These new endeavours are generally collectively referred to as the *postscaling technology* [13]. This includes the introduction of new materials for high mobility channels or high-dielectric insulators, new transistor structures such as FinFETs [14], new technologies to increase the integration of devices, such as 3D integration [15] and even the incorporation of new functions into CMOS devices, such as using the response of electrons spin to a magnetic field or to light [16, 17].

In order to improve the charge carrier mobility of MOSFETs channels, strain engineering was already put into use around 2003 with Si and the

90 nm technology node [18, 19]. The introduction of mechanical strain alters the crystal symmetry of the semiconductor and the resulting band structure, which may lead to an increase of the carrier mobilities. Such a modification of the transport properties can also be the result of reduced electron or hole effective masses, or of a reduction in carrier scattering, which is a main cause of boosted carrier mobilities.

Among the materials envisioned in the context of this postscaling technology for even higher mobility channel transistors, the semiconducting alloy GeSn is a very promising candidate. Its direct bandgap also paves the way for group-IV integrated long-wavelength optoelectronic applications.

Problem statement and objectives of this work

Empowered by the renewed interest for GeSn, several research laboratories have recently achieved the successful fabrication of epitaxial layers with high crystalline quality [4, 20, 21]. Although the structural properties of such materials have simultaneously been investigated in many studies, few extensive analyses of the transport properties of GeSn materials have been performed. This new material possesses characteristics that are not usually found in other group-IV materials, namely its much lower bandgap and the crystalline defects resulting from the introduction in a Ge matrix of large Sn atoms, which easily segregate or precipitate. These crystalline defects generally act as electronic traps and directly alter the desired improved performances of devices made out of these materials. The relevance of routine electrical characterization techniques to determine the traps density, such as the conductance method, are also questioned. Several issues are indeed encountered as a consequence of the lower bandgap, which leads to an increased inversion response in MOS structures and can impair the accurate evaluation of the traps concentration.

This work is therefore dedicated to the *assessment of the impact of electron traps on the transport properties of GeSn materials.*

Within the framework drawn by the statement of this general objective, the following questions will be addressed in this thesis:

- What is the overall impact of the presence of traps states on the electrical characteristics fundamental devices such as GeSn-based diodes ?
- Can some of the traps properties be evaluated from the electrical characterization of such diodes ?

- What is the impact of the lack of passivation in the case of mesa diodes with exposed surfaces ?
- Can the conductance method still provide an accurate estimation of the density of interface traps D_{it} in GeSn materials, in spite of the low bandgap energy and the enhanced inversion response in MOS capacitor structures, which are test vehicles for advanced modern devices ?
- What is the effect of the bandgap energy, carrier mobilities and effective masses on the onset of the inversion response ?

In order to provide answers to these important questions, the complete electrical characteristics of Boron-doped p-GeSn/n-Ge pn junction diodes will be analyzed using current-voltage and capacitance-voltage measurements, also as a function of temperature. Theoretical analysis based on the full harnessing of a home-built numerical simulation tool will give access to many microscopic quantities such as the current densities, the electric field and the local carrier concentrations. The use of this tool to reproduce the experimental data will allow to obtain quantitative information on the traps properties found in the diodes. Next, current-voltage and current transients measurements will serve in the investigation of the behaviour of unpassivated mesa diodes. The construction of an equivalent electric circuit model will provide further insight into the time constants involved in those transients.

The simulation of the complete admittance response of GeSn MOS structures will subsequently set the foundation for the analysis of the effects of interface traps on typical features usually found in C-V characteristics. Based on that admittance response, the consequences of the low bandgap energy of GeSn materials on the application of the conductance technique will be assessed and various interface traps energies, distributions and densities will be explored. Finally, the numerical simulation of the admittance response as a function of bandgap energy, majority and minority carrier mobilities and effective masses will result in the determination of their specific influence on the strength of the inversion response.

Among the methods of characterization of interface traps, many are based on admittance. Those are indeed very efficient, as the sensitivity of the conductance method, e.g., can detect defects with as low as a 10^9 cm^{-2} density [22]. Methods for detecting the atomic elements responsible for the interface traps such as Angle Resolved X-ray Photoelectron Spectroscopy (ARXPS) or Electron Spin Resonance (ESR) can at best detect densities at

least one order of magnitude larger than that level and are therefore unsuitable for our goal. Deep Level Transient Spectroscopy (DLTS) [23, 24, 25, 26] is another well established technique that has a very high sensitivity. The accurate interpretation of its results requires a strong expertise of the technique, though, and it was not our goal to replicate the excellent work already performed using the DLTS method by other research groups [27, 28]. The results from complementary studies performed with DLTS will instead be used as reference and will be compared to our work [28, 29].

Content structure

This work is organized in the way described here below.

Chapter 2 discusses the characteristics of $Ge_{1-x}Sn_x$ alloys. The challenges pertaining to the growth of $Ge_{1-x}Sn_x$ layers by Molecular Beam Epitaxy (MBE) and Chemical Vapor Deposition (CVD) are reviewed. The effect of Sn alloying on the Ge band structure and the resulting properties are then considered. Direct applications of $Ge_{1-x}Sn_x$ materials to high-mobility transistors and photoelectronic applications are also presented.

Methods of experimental characterization are discussed in **Chapter 3**. The techniques pertaining to the characterizations of pn junctions are introduced, followed by the general principles of impedance spectroscopy and characterization methods applicable to MOS structures.

The principles of the numerical simulation tool used in this work are developed in **Chapter 4**. The equations and hypotheses constitutive of the model are detailed and the numerical procedure for the computation of the solution is presented, both under steady-state and small-signal regimes.

In **Chapter 5**, the results related to the electrical characterization of pn GeSn/Ge diodes are presented. Their current-voltage (I-V) and capacitance-voltage (C-V) characteristics are analyzed in view of assessing the impact of electron traps at the GeSn/Ge interface. The presence of such traps is highlighted by the measurements and numerical simulations allow to obtain quantitative information on the energy of those traps. The effect of the lack of passivation of mesa diodes on their I-V characteristics and current transients is also thoroughly explored.

Chapter 6 details the results obtained from the theoretical investigation of the effect of electron traps on GeSn materials in MOS structures. Their effect on C-V characteristics and on the application of the conductance method are extensively examined. The impact of the GeSn materials

properties such as lower bandgap on the inversion response of minority carriers is reported. Experimental characteristics of GeSn MOS devices are also described and linked to the previous numerical observations.

Finally, general conclusions of this work are presented in **Chapter 7** along with perspectives and suggestions for future work.

Chapter 2

GeSn, a group-IV semiconducting alloy

2.1 Motivations

GeSn is a semiconducting alloy with many very interesting electronic and optoelectronic characteristics that make it attractive as a new material for improved performance devices and new optoelectronic applications. GeSn alloys exhibit several beneficial perspectives that allow:

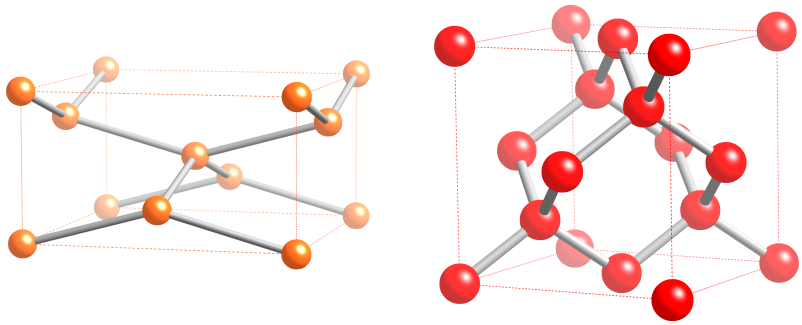
- Strain engineering as a stressor for Ge;
- Energy bandgap engineering by controlling the Sn content;
- Direct bandgap material for group-IV integrated photonic applications;
- Reduced crystal growth temperature due to the low temperature required for Ge and Sn to mix together homogeneously (eutectic point).

In this Chapter, the open challenges regarding the growth of $Ge_{1-x}Sn_x$ alloys are presented. The energy band structure and electronic properties of $Ge_{1-x}Sn_x$ are then reviewed, especially the direct bandgap crossover and carrier mobility properties. Finally, applications of $Ge_{1-x}Sn_x$ compounds for next generation high mobility MOSFETs and long wavelength optoelectronic devices are discussed.

2.2 Growth methods

2.2.1 $Ge_{1-x}Sn_x$ crystalline structure and growth challenges

$Ge_{1-x}Sn_x$ is a very challenging semiconductor material to produce. Pure Sn generally displays a metallic behaviour, when it is in the β-Sn form. But it becomes a semiconductor, α-Sn, for temperatures below 13.2°C [1]. Its crystalline structure then goes from a body-centered tetragonal form (Fig. 2.1 (a)) to a face-centered diamond-like cubic crystal structure (Fig. 2.1 (b)), identical to that of crystalline silicon and germanium.



(a) (b)

Figure 2.1: Crystal structure of (a) β-Sn: body-centered tetragonal and (b) α-Sn: diamond-like face-centered cubic.

The Ge-Sn binary system is an eutectic alloy, which means that both atom species form a non-ordered homogeneous solid mix and combine into a joint superlattice. The thermal equilibrium solid solubility of Sn in the Ge matrix at 500°C is as low as 1 atomic % [2, 3]. The eutectic temperature is 231.1°C (see the phase-diagram in Fig. 2.2), which implies that it is very difficult to increase the Sn content in $Ge_{1-x}Sn_x$ layers. Sn precipitation indeed easily occurs during the growth process, even at low temperature[1]. This is in strong contrast with $Si_{1-x}Ge_x$ alloys, where the Si-Ge binary system has a complete solid solubility, allowing to use any ratio of Si and Ge [30].

In the fabrication of $Ge_{1-x}Sn_x$ thin films, precipitation of Sn is regularly observed, which consists in Sn atoms withdrawing from the GeSn matrix to

[1]Low temperature, in this context, is to be compared with the growth temperature for thick Si films of 1000°C.

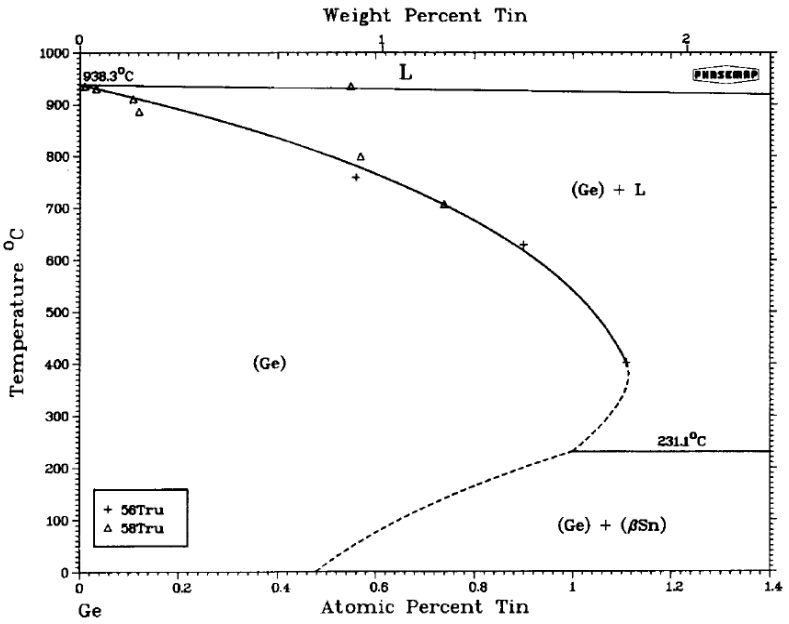


Figure 2.2: Enlarged view of the Ge-Sn phase diagram for 0 to 1.4 at.% Sn, after [31].

form all-Sn clusters. This can occur both during the growth or subsequent thermal processes [32, 33]. Out of thermal equilibrium methods such as low temperature processes or strain engineering of the thin films are therefore necessary to produce high quality $Ge_{1-x}Sn_x$ layers. Sn segregation, a non-homogeneous distribution of the Sn atoms in the Ge matrix, was also reported during the oxidation of $Ge_{1-x}Sn_x$ layers. Oxidation of $Ge_{1-x}Sn_x$ indeed boosts the Sn diffusion, resulting in an increase of the Sn content near the surface [34].

The desired strain effects from GeSn materials require the growth of epitaxial layers. There are many epitaxy techniques, such as Liquid Phase Epitaxy, Solid Phase Epitaxy, Vapor Phase Epitaxy or Molecular Beam Epitaxy. However, two particular techniques are mostly used to produce epitaxial $Ge_{1-x}Sn_x$ alloys: Molecular Beam Epitaxy (MBE) and Chemical Vapor Deposition (CVD). Both of these methods are briefly presented below along with their current achievements and issues in the fabrication of $Ge_{1-x}Sn_x$ layers.

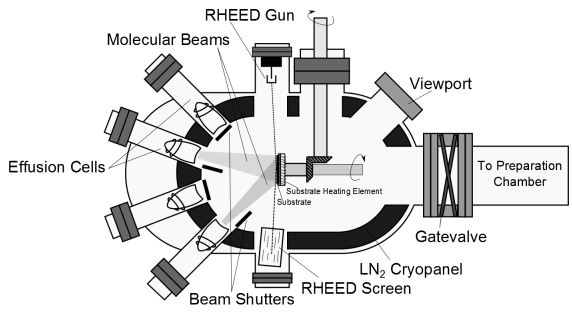


Figure 2.3: Schematic illustration of an ultra-high-vacuum chamber for MBE. More details can be found in Ref. [36].

2.2.2 Molecular Beam Epitaxy

Molecular Beam Epitaxy [35, 36], schematically depicted in Fig. 2.3, has been extensively used to produce the first $Ge_{1-x}Sn_x$ layers [37, 38, 39]. The technique is based on heating the ultra-pure form of the solid elemental sources until they undergo sublimation and then condense on the substrate to form the epitaxial layer. The "beam" term in MBE refers to the fact that the evaporated atoms do not interact with each other because of the ultra high vacuum (UHV) environment of the chamber, which results in long mean free paths for the atoms. Reflection high energy electron diffraction (RHEED) [40, 41], based on the observation of the diffraction pattern from the reflection of electrons beamed on the sample surface, is routinely used for in-situ monitoring of the growth and surface morphology of the layers. Auger electron spectroscopy (AES) [42] or X-ray photoelectron spectroscopy (XPS) [43, 44] can also be used to analyze the composition of the surface during the growth. All these in-situ characterization resources allow to monitor the crystal quality during the deposition process while enabling comprehensive analysis of the growth mechanisms.

The first GeSn layers were grown by MBE on quasi lattice matched III-V materials, with up to 27% Sn content [37], although lots of extended defects were present in the layers [39]. Later, growth of GeSn on group IV semiconductors was also achieved [45], a step closer to the anticipated integration of GeSn materials with Si technology.

MBE growth of GeSn layers suffers from usually high point defect densities, though, because of the low adatom mobility on the growth surface [46], and of Sn segregation. The required UHV and low growth rates also make it unlikely to be suitable for an economical mass industrial production. MBE

remains the method, however, that is able to achieve the highest Sn concentrations, up to 25% (on Si) and 20% (on Ge) [47].

2.2.3 Chemical Vapor Deposition

Chemical vapor deposition [48, 49] is an extensively used technique to deposit thin films of semiconductors by submitting a heated substrate to a flow of vapor-phase precursors. These precursors are made of the elements to be deposited and chemically react or decompose on the substrate surface to form the intended deposit.

A CVD system is typically composed of a reaction chamber with in-let and out-let gas lines valves, equipped with mass flow controllers to regulate the amount of gas delivered to the chamber. Heating elements are also necessary, in order to heat the whole chamber or only the substrate, depending on the exact CVD method in use. The basic steps of the CVD growth process are as follows:

- Controlled amounts of vapor-phase precursors are injected inside the reaction chamber, along with carrier gases such as H_2, N_2 or Ar;
- The gas precursors diffuse to the substrate;
- The gas precursors are adsorbed on the surface and react chemically;
- The extra atoms lying on the surface, or adatoms, migrate until they become part of the lattice;
- The volatile by-products desorb and diffuse towards the exhaust gas lines.

CVD allows for deposition far from equilibrium growth conditions, which is useful for the growth of $Ge_{1-x}Sn_x$ in order to avoid Sn segregation and precipitation. Moreover, the CVD technique is able to grow films uniformly on large wafers and also to process multiple substrates simultaneously, which makes it closer to the requirements of mass production required by large scale manufacturers.

However, growing $Ge_{1-x}Sn_x$ layers using CVD is not without complications, which probably explains why MBE grown $Ge_{1-x}Sn_x$ was initially more popular. Contrary to the growth of Si and Ge, where the corresponding hydrides, Si_nH_{2n+2} and Ge_nH_{2n+2}, are used as precursor gases without notable difficulty, Sn hydrides are unstable at room temperature because of the weaker Sn-H chemical bonds. SnH_4 is a highly unstable compound and

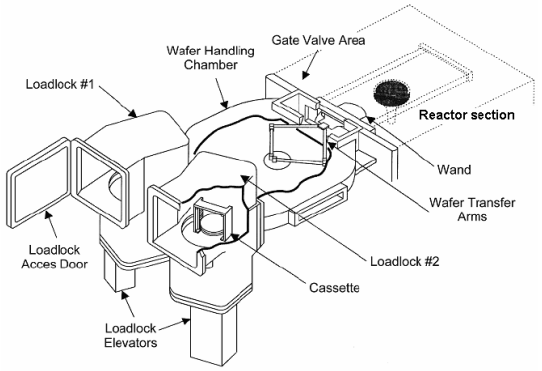


Figure 2.4: Schematic representation of the ASM Epsilon® 2000, a typical industrial tool used for the growth of $Ge_{1-x}Sn_x$ layers by CVD (source: ASM).

is also extremely toxic, for instance. The group of Kouvetakis *et al.* suggested the use of the heavier deuterium to replace hydrogen [50, 51]. Using SnD_4 as gas precursor, they were indeed able to produce $Ge_{1-x}Sn_x$ layers with up to 15% Sn. However, SnD_4 is still highly unstable and utterly toxic, even though it is less so than SnH_4.

Another gas precursor for the Sn component, $SnCl_4$, has later been used by Vincent *et al.* [20]. It is completely stable and commercially available, actually delivered as a liquid at room temperature. The addition of a H_2 bubbler is therefore necessary to provide the precursor under vapour phase to the CVD reactor. Epitaxial growth of $Ge_{1-x}Sn_x$ layers at 320°C with up to 8% Sn has been achieved under these conditions.

The $Ge_{1-x}Sn_x$ samples discussed in Chapters 5 and 6 have been fabricated using this CVD method in IMEC [52, 20]. An ASM EPI cluster tool, the Polygon® 8200 has been used for the growths. This EPI reactor is similar to the ASM Epsilon® 2000, schematically depicted in Fig. 2.4, which is an horizontal cold-wall, load-locked single-wafer reactor. This chamber design implied that only the substrate is heated, which is performed through radiation by set of infrared lamps. The advantage of this setup is to reduce the deposition on the chamber walls. The substrates are usually rotated during the growth to ensure an homogeneous thickness.

2.3 $Ge_{1-x}Sn_x$ energy band structure and electronic properties

2.3.1 Direct bandgap

Ge is an indirect bandgap material because the minimum energy of its conduction band and the maximum energy of its valence band are not located at the same point in momentum space. The maximum energy of its valence band is indeed located at the Γ-point in the Brillouin zone, whereas the minimum energy of its conduction band is at the L-point. The indirect bandgap energy of Ge is 0.66 eV at room temperature (RT), lower than the Si indirect bandgap which is about 1.12 eV at the same temperature range.

Alloying Ge with Sn significantly alters the band structure of Ge and confers novel properties to the resulting material. The bandgap energy of GeSn indeed decreases below that of pure Ge as the Sn content is increased. The conduction band edge at the Γ-point also drops faster than at the L-point, as depicted in Fig. 2.5. At RT, the conduction band edge of Ge at the Γ-point is 0.14 eV above that at the L-point. With the addition of Sn in the $Ge_{1-x}Sn_x$ alloy, the energy difference between the two decreases, until the Γ-point becomes lower than the L-point. At this stage, it is the minimum among all other valleys in the band structure, as well. This makes the GeSn alloy with such a Sn content a direct bandgap semiconductor. The indirect to direct bandgap crossover is expected to occur for a Sn content of about 9%[4].

The direct bandgap in $Ge_{1-x}Sn_x$ alloys is expected to result in a significant enhancement of photoemission as well as photon absorption, paving the way for a new class of infrared devices. As these are based on group IV materials, they can therefore be directly integrated into Si technology, contrary to other III-V direct bandgap materials whose integration is not as straightforward.

Not only the Sn content but also the strain in $Ge_{1-x}Sn_x$ epitaxial layers has an impact on the energy band structure and therefore on the bandgap. These dependences of the energy bandgap and energy band structure on the strain in addition to the Sn content have been observed by spectroscopic ellipsometry [54, 55], optical transmittance spectroscopy [56], Fourier transform infrared spectroscopy [57] and photoluminescence [58, 59, 60]. The reported consequence of compressive strain is that the Sn content necessary to reach the direct-indirected crossover is increased, and conversely decreased under tensile strain [61].

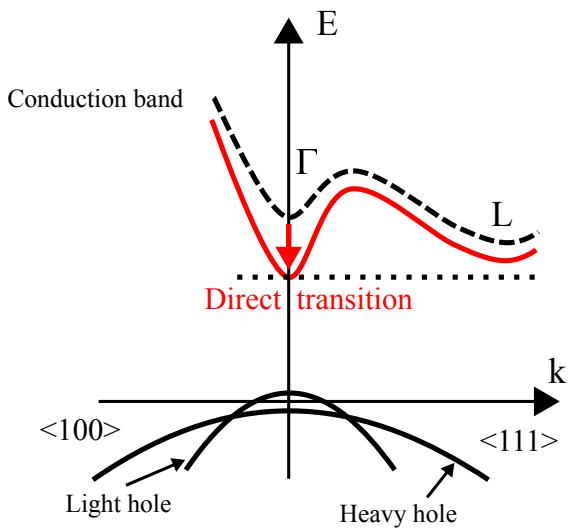


Figure 2.5: Schematic energy band structure change from an indirect to a direct bandgap for Sn content over 9% [53].

2.3.1.1 Vegard's law

Vegard's law [62] states that the relaxed lattice constant a_0 of a crystal alloy $A_{1-x}B_x$ can be empirically estimated by a weighted linear interpolation between the lattices of its constituents A and B:

$$a_0^{A_{1-x}B_x} = a_0^{\mathrm{A}}(1-x) + a_0^{\mathrm{B}}x \tag{2.1}$$

where $a_0^{A_{1-x}B_x}$, a_0^{A} and a_0^{B} are the relaxed lattice constants of the $A_{1-x}B_x$ alloy, of A and of B, respectively. The bandgap energy of a semiconductor compound is generally closely related to the lattice constant and can therefore be estimated using a similar relationship [63].

Figure 2.6 shows the dependence of the direct and indirect bandgaps in $Ge_{1-x}Sn_x$ as a function of Sn content x, calculated from a linear interpolation of the Ge and α-Sn bandgaps. According to this linear model, an indirect to direct crossover would therefore occur for Sn contents around $x = 21\%$, well beyond the experimentally estimated value of $x \approx 8-9\%$ reported earlier.

This discrepancy is probably mostly related to the large 16% lattice mismatch between Ge and α-Sn [30], which induces a significant local strain around the Sn atoms, and results in a deviation from the simple linear

relationship. The introduction of a so-called bowing parameter b^{GeSn} into Eq. (2.1) allows to account for this difference,

$$a_0^{\mathrm{Ge}_{1-x}\mathrm{Sn}_x} = a_0^{\mathrm{Ge}}(1-x) + a_0^{\mathrm{Sn}}x + b^{\mathrm{Ge}_{1-x}\mathrm{Sn}_x}x(1-x). \tag{2.2}$$

Various values of the bowing parameters have been reported from theoretical calculations, $b^{\mathrm{GeSn}} = 0.063$ Å [64], 0.65 Å [53], 0.0468 Å [65] and experimental observations $b^{\mathrm{GeSn}} = 0.166$ Å [64], -0.066 Å [65], 0.221 Å [66] and 0.0435 Å [67]. The discrepancies in those values are mostly related to experimental uncertainties in the exact GeSn composition and strain level.

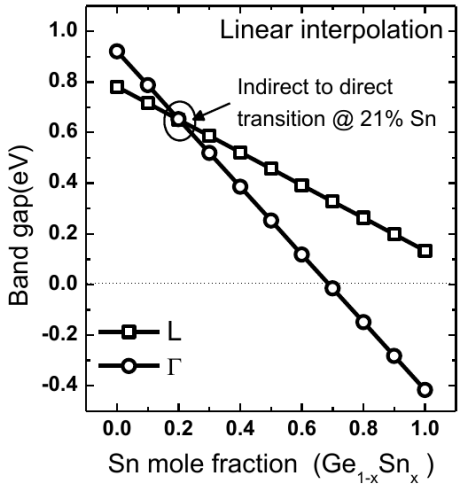


Figure 2.6: Dependence of the direct (Γ) and indirect (L) bandgaps in $\mathrm{Ge}_{1-x}\mathrm{Sn}_x$ on the Sn content, calculated from a linear interpolation between the bandgaps of Ge and α-Sn[68].

2.3.2 Carrier mobility boost in Ge

As discussed in the Introduction, several materials are being explored for their high mobility properties, as this directly improves the power-performance ratio of the corresponding MOSFETs, as well as their switching speed capability. Table 2.1 summarizes the electron and hole mobilities, effective masses and bandgaps of some of them. Binary III-V compounds such as GaAs, InP, InAs and InSb have very high electron mobilities. The bulk electron mobilities in GaAs and InSb are approximately 6 and 50 times larger than in Si, respectively. The hole mobility of InSb, however, is for

Parameter	Si	Ge	GaAs	InP	InAs	InSb
Electron mobility [cm^2/Vs]	1450	3800	9000	5400	33000	70000
Transverse electron effective mass [m_T^*/m_0]	0.19	0.082	0.066	0.073	0.023	0.014
Longitudinal electron effective mass [m_L^*/m_0]	0.916	1.59				
Hole mobility [cm^2/Vs]	505	1800	400	190	450	850
Heavy hole effective mass [m_{HH}^*/m_0]	0.55	0.28	0.45	0.45	0.57	0.44
Light hole effective mass [m_{LH}^*/m_0]	0.15	0.044	0.082	0.12	0.35	0.016
Bandgap [eV]	1.12	0.66	1.42	1.34	0.35	0.18

Table 2.1: Electronic properties of high mobility material candidates: electron and hole mobilities and effective masses. [75, 76, 77]

instance less than double that of Si, although it is the III-V compound with the highest hole mobility.

Hole mobility in Ge is higher than any III-V materials and almost four times higher than Si. Its electron mobility is also 2.5 times higher than that of Si. Ge MOS transistors with high channel mobilities have already been reported, with peak electron mobilities of 1020 cm^2/Vs [69] and peak hole mobilities of 725 cm^2/Vs [70, 71]. Their performance, though higher than plain Si devices, does not outperform current "state of the art" strained Si devices. The development of strained Ge channels therefore seems to be the way to go to obtain mobilities that can outperform Si and SiGe based devices, as indicated by theoretical calculations of carrier mobilities under compressive uniaxial or biaxial strain [72, 73, 74].

$Ge_{1-x}Sn_x$ and its lattice constant larger than Ge, depending on the Sn content, allows to induce such a strain level in a Ge channel and further improve the carrier mobility. Doubling of the mobility in Ge channel can be reached for both holes and electrons by applying strain, with an increase in hole mobility up to one order of magnitude expected under the application of 1% tensile strain [78].

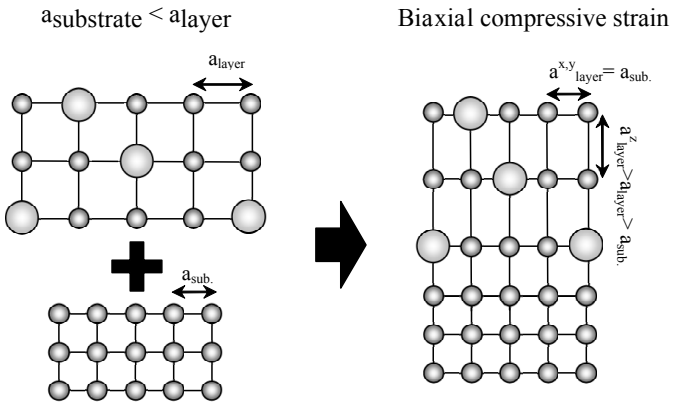


Figure 2.7: Schematic representation of a lattice mismatch leading to biaxial compressive strain. From [79].

In addition, $Ge_{1-x}Sn_x$ layers themselves might see their electron mobility improve with the increase in Sn content as well. The effective mass of electrons at the Γ-point is indeed smaller than at the L-point. When the Sn content depresses the edge of the Γ-point lower than the L-point, electrons with this smaller effective mass become available, and the electronic mobility improves accordingly.

2.4 $Ge_{1-x}Sn_x$ applications

Many applications are envisioned for $Ge_{1-x}Sn_x$ materials, which can be subdivided into stressors or strained materials for high mobility CMOS devices and long wavelengths photoelectronic applications, both of which are described in this section.

2.4.1 High mobility CMOS devices

2.4.1.1 $Ge_{1-x}Sn_x$ stressor for Ge channels MOSFETs

The first use of $Ge_{1-x}Sn_x$ as a stressor is to produce uniaxial compressive strain in a Ge pMOS device (see Fig. 2.7). As has already been done with Si devices, replacing the source and drain (S/D) of MOSFETs by a material with a larger lattice constant results in an uniaxially compressively strained channel (Fig. 2.8 (a)). $Ge_{1-x}Sn_x$ is therefore a material of choice for such an application [80].

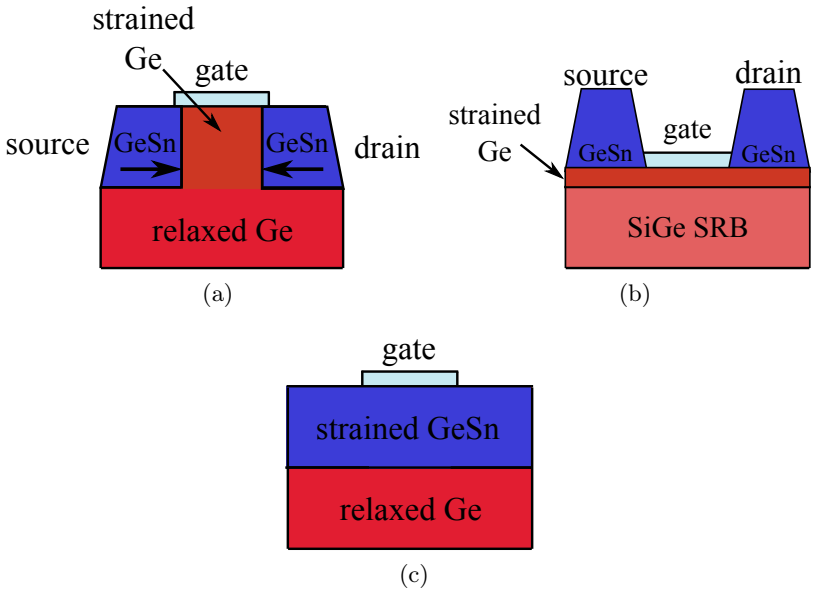


Figure 2.8: High mobility CMOS devices configurations: (a) strained Ge with GeSn S/D stressors, (b) strained Ge on top of SiGe SRB with GeSn S/D stressors and (c) compressively strained GeSn channel on top of Ge.

Another device configuration is to use a SiGe Strain Relaxed Buffer (SRB) on top of which the Ge channel is fabricated, so as to already induce biaxial compressive strain in the Ge layer (Fig. 2.8 (b)). This configuration is already able to produce large channel stress, and Ge S/D also act as stressors because of the lattice mismatch with the SRB. Using $Ge_{1-x}Sn_x$ S/D instead of just Ge would therefore further improve the strain and subsequently the channel mobility of such a device. This arrangement is more advantageous than uniaxial compressive strain with $Ge_{1-x}Sn_x$ S/D only because the SiGe SRB and its already smaller lattice constant improve the strain transfer from the $Ge_{1-x}Sn_x$ S/D to the Ge channel. Moreover, as the level of strain applied to the channel is dependent on the lattice mismatch between the S/D and the SRB, the Sn content can be reduced while maintaining a sufficient level of stress in the channel. The lower Sn concentration required decreases the difficulties related to the growth of $Ge_{1-x}Sn_x$ materials with a high Sn content.

2.4.1.2 Compressively-strained $Ge_{1-x}Sn_x$ and tensile-strained Ge channels

Another category of devices where $Ge_{1-x}Sn_x$ materials might prove valuable is compressively strained $Ge_{1-x}Sn_x$ and tensile strained Ge channels (Fig. 2.8 (c)). In both these devices, the mobility of both holes and electrons are enhanced [78, 81]. Strained $Ge_{1-x}Sn_x$ channels pMOSFETs have already been reported, with Sn concentrations of 3% to 5% and improved performances [82, 83]. The use of $Ge_{1-x}Sn_x$ to obtain relaxed virtual substrates with a large lattice constant is favored over III-V materials because of the absence of auto doping issues [21, 84, 85].

$Ge_{1-x}Sn_x$ layers were grown by MBE that are able to induce biaxial tensile strain up to 0.71% in Ge layers [86]. Using UHV-CVD, tensile strained Ge was fabricated using $Ge_{1-x}Sn_x$ grown with Ge_2H_6 and SnD_4 as gas precursors. Tensile strain of 0.43% with a Sn content in the SRB of just 3.5% is reported [85].

On the electron mobility side, n-channel MOS devices were also recently fabricated using compressive strained $Ge_{0.976}Sn_{0.024}$ [87] and $Ge_{0.95}Sn_{0.05}$ [88] as channel material on relaxed Ge, grown by MBE or CVD, respectively.

2.4.2 Optoelectronic applications

As a straightforward consequence of its tunable direct bandgap, many optoelectronic applications based on $Ge_{1-x}Sn_x$ materials are reported, such as photodiodes, lasers, LEDs and photovoltaic cells. Direct integration on the Si technology platform and with other group IV semiconductors is a tremendous advantage of these applications.

Light emitting or detecting devices

The tunable bandgap decreasing with higher Sn content extends the IR wavelength range available with Ge photoelectronic devices. The indirect to direct crossover for Sn content over approximately 9% greatly improves the photoresponse and absorption. $Ge_{1-x}Sn_x$ can also be used to produce sufficient tensile strain on a Ge layer, giving rise to a direct bandgap in the Ge layer as well.

$Ge_{1-x}Sn_x$ photodetectors have a better photoresponse at longer wavelengths, increasing with the Sn content, as reported in [89, 90, 91] (see Fig. 2.9 for a schematic view of such a photodetector). A photodetector based on a $Ge_{1-x}Sn_x$/Ge quantum well has been fabricated [92] and

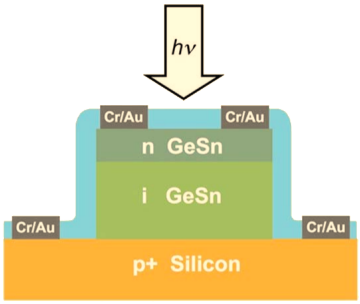


Figure 2.9: Schematic view of a GeSn photodiode stack under light application. From [89].

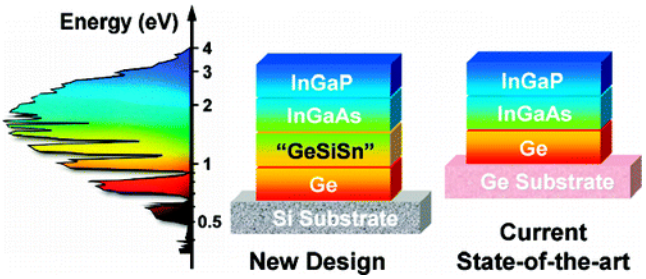


Figure 2.10: (a) Improved solar spectrum absorption with (b) a new photovoltaic design using high-efficiency hybrid multijunction solar cell with the addition of a GeSiSn layer and (c) current state-of-the-art Ge/InGaAs/InGaP device. From [100].

a $Ge_{1-x}Sn_x$ heterojunction LED on a Si substrate has also been demonstrated [93]. Theoretical calculations for lasers based on $Ge_{1-x}Sn_x$ and $Si_{1-x-y}Ge_ySn_x$ have been performed [94, 95, 96, 97, 98] and a practical observation of lasing in $Ge_{1-x}Sn_x$ on a Ge virtual substrate has been reported [99].

Energy harvesting devices

Beyond $Ge_{1-x}Sn_x$, ternary alloys such as $Si_{1-x-y}Ge_ySn_x$ are also proposed for solar cell applications, as a buffer layer for multi-junction solar cells composed of III-V compounds [100]. A $Si_{1-x-y}Ge_ySn_x$ layer, lattice matched to a Ge substrate and with a bandgap energy around 1 eV, is a suitable buffer layer for an $In_{1-x}Ga_xAs$ layer [101] used in such devices, as shown in Fig. 2.10.

Chapter 3

Electrical characterization methods

With the exploration of new materials like $Ge_{x-1}Sn_x$ arises the need for a complete and accurate characterization of their electrical transport properties. Many experimental tools can be used in this regard and the main experimental techniques used in this work are described in this Chapter. Characterization methods involving frequency-dependent and temperature-dependent measurements are discussed here.

In Section 3.2, the characterization techniques used to assess the properties of both Schottky metal-semiconductor contact diodes and p-n semiconductor diodes using current-voltage and capacitance-voltage measurements are introduced. Section 3.3 presents the general principles of impedance and admittance measurements. Modeling with an equivalent electrical circuit and the connection with physical processes is exposed. Characterization techniques pertaining to MOS structures are detailed in Section 3.4. The ideal admittance behaviour of these structures is first recalled, followed by a presentation of the conductance method, used to extract the trap density at the interface between the semiconductor and the oxide. Various effects that can potentially hinder those measurements are listed and discussed. Finally, Section 3.5 discusses the experimental setup used in this work.

3.1 Introduction

The electrical transport properties of semiconducting materials are at first dependent on the chemical composition of the crystal material they are made of. This determines properties such as the bandgap of the material, the effective masses of the carriers or the dielectric constant. In the case of compound semiconductor materials, such as $Ge_{x-1}Sn_x$, a whole range of different properties can be obtained depending on the proportion of each constituent, *e.g.* reaching a direct bandgap for some value of Sn concentration. These properties are also affected by lattice defects or chemical impurities that can be present and lead to the appearance of additional energy states within the bandgap.

The properties of semiconductor materials can be hugely influenced by even very small concentrations of those defects or impurities. Semiconductor characterization techniques strive to detect those concentrations and assess their impact on the electrical characteristics of devices. All electronic properties of semiconducting materials could theoretically be obtained by an exhaustive determination of the chemical and structural characteristics of the materials. Unfortunately, this cannot be done in practice [102]. One therefore has to resort to a limited set of characteristics, obtained through various characterization techniques, to try and sketch a picture of the structural and electronic properties of the material under investigation. Although inherently incomplete, this picture allows to better understand the link between microscopic physical parameters and macroscopic electrical properties. This comprehension of the underlying phenomenons related to distinctive resulting properties is of paramount interest for the design, development and improvement of semiconducting devices.

To investigate the experimental transport properties of semiconductors, an external stimulus is generally provided to the semiconducting structure and the subsequent response is analyzed. The stimulus can be, *e.g.*, a known electrical bias, current or even optical excitation, and the response will be the resulting current or voltage. As a consequence of the external excitation, a huge number of fundamental microscopic processes will take place and lead to the global electrical response. Those processes include, but are not limited to, the transport of charge carriers through the bulk of the semiconductor, the crossing of interfaces, the trapping of charges, the generations and recombinations processes and the injection mechanisms at metal contacts.

3.2 Schottky diodes and pn junctions

3.2.1 I-V characterization

Current-Voltage (I-V) measurements performed on either pn or Schottky diodes allow to obtain information on the transport mechanisms such as the reverse saturation current I_0 and the ideality factor n, which is related to the amount of recombinations occurring in the semiconductor. With Schottky diodes, it also allows to extract the barrier height ϕ_b. Even though the internal mechanisms are different for Schottky diodes and pn junctions, the relationship between the current I and applied bias V in both cases takes the same form

$$I = I_0 \left(e^{\frac{qV}{kT}} - 1 \right), \tag{3.1}$$

where I_0 is the reverse saturation current, q is the electron charge, k is the Boltzmann constant and T is the temperature. In the case of a pn junction, I_0 is given by the Shockley's equation [103]

$$I_0 = \frac{qD_p}{L_p}\frac{n_i^2}{N_D} + \frac{qD_n}{L_n}\frac{n_i^2}{N_A}, \tag{3.2}$$

where $D_{p,n}$ are the holes and electrons diffusion coefficients, respectively, $L_{p,n}$ are the diffusion lengths for holes and electrons, n_i is the intrinsic carrier concentration and N_A and N_D are the acceptors (on the p-side) and donors (n-side) concentrations, respectively.

For a Schottky diode, the reverse saturation current is dependent on thermionic emission over the barrier ϕ_b as [104]

$$I_0 = A^* A T^2 e^{-\frac{q\phi_b}{kT}} \tag{3.3}$$

where A^* is the effective Richardson constant, A is the surface area of the contact and ϕ_b is the barrier height. The effective Richardson constant for thermionic emission, neglecting the effect of optical phonon scattering [105, 106] and quantum mechanical reflection of electrons by the Schottky barrier [107, 108, 109], is dependent on the electron effective mass m_e^* as

$$A^* = \frac{4\pi q m_e^* k^2}{h^3} \tag{3.4}$$

where h is Planck's constant. This relation is only valid when emission of electrons over the barrier is the dominant process. For real devices, though, the relationship between current and applied bias does not follow exactly Eq. (3.1). Recombination of carriers, variation of the barrier height with

applied bias and the presence of interface states can affect this relationship. The *ideality factor* n, a parameter accounting for the departure from ideality, is inserted in Eq. (3.1), leading to

$$I = I_0 \left(e^{\frac{qV}{nkT}} - 1 \right). \tag{3.5}$$

An equivalent ideality factor is inserted in the current equation for pn junctions to account for non-idealities, which are attributed to recombinations [110]. The ideality factor is comprised between $n = 1$ (ideal case) where the only current source is the diffusion current and $n = 2$, where the recombination current dominates the total current I.

For relatively large applied biases, $V > 3kT/q$, Eq. (3.5) can be approximated for both Schottky diodes and pn junctions by

$$I = I_0 \, e^{\frac{qV}{nkT}}, \tag{3.6}$$

In this situation, a logarithmic plot of $\ln(I) = \ln(I_0) + \frac{qV}{nkT}$ as a function of V therefore leads to a straight line when forward bias is applied. This allows to determine the ideality factor and the reverse saturation current, from which the barrier height ϕ_b of a Schottky diode can be deduced if the effective Richardson constant is known. If it is not, I-V measurements performed at various temperatures allow to separate the effective Richardson constant from the barrier height value. Indeed, from Eq. (3.3), an Arrhenius plot of $\ln(I_0/T^2)$ as a function of $q/(kT)$ will give a straight line, the slope of which is equal to ϕ_b and the x-intercept equals to $\ln(A^*)$.

Series resistance effect

Schottky diodes and pn junctions can also be further driven away from the ideal behaviour by the presence of a non-negligible series resistance R_s. This series resistance originates from the bulk resistivity of the semiconductor and can be especially prominent if the substrate is particularly thick or lowly doped. Contact resistance, sometimes due to non-perfect ohmicity of the deposited metal, and even the external circuit's wires can impact the final value of R_s. In the presence of non-negligible R_s, there is a potential drop over the bulk of the device and/or the contacts. The applied bias V is therefore not entirely applied to depletion region of the junction, and Eq. (3.6) is rewritten as

$$I = I_0 \, e^{\frac{q(V - IR_s)}{nkT}}. \tag{3.7}$$

The immediate consequence on the forward current is that the exponential growth of I with applied bias becomes linear for some forward value of V. The slope in forward regime of a logarithmic plot of $I(V)$ does not directly yield the ideality factor and reverse saturation current I_0 values, anymore. Particular caution to the onset of current limitation due to the series resistance must therefore be paid. If so, the range of potentials on which to calculate the slope of $\ln(I)$ vs V will be restricted to ensure that relation (3.6) is still valid.

3.2.2 C-V characterization

Capacitance-voltage (C-V) measurement of a Schottky diode or pn junction under reverse bias is a common technique used to determine the doping concentration of the semiconductors and the barrier height of a Schottky diode [111, 102, 112]. Starting with the example of an ideal n-type Schottky diode without interface states, the application of a steady reverse bias $V < 0$ leads to the formation of a depletion region whose width W_d is

$$W_d = \sqrt{\frac{2\epsilon_r \epsilon_0 (V_d - V)}{qN_D}} \tag{3.8}$$

where ϵ_r is the semiconductor dielectric constant, ϵ_0 is the vacuum permittivity, V_d is the built-in potential corresponding to the barrier seen by conduction electrons in the semiconductor, and N_D is the doping concentration in the semiconductor. The superimposed ac bias used to measure the capacitance will modulate the total applied bias V from $V - V_{\mathrm{ac,max}}$ to $V + V_{\mathrm{ac,max}}$, which will in turn modulate the width of the depletion region around the value W_d, from $W_d + \Delta W_d$ to $W_d - \Delta W_d$ (see Fig. 3.1). The charge modulation resulting from the space charge increasing and decreasing at the edge of the depletion region will result in a capacitance that can be measured. The small-signal definition of the capacitance in ac regime is indeed the ratio of the differential charge to differential applied voltage

$$C = \frac{\mathrm{d}Q}{\mathrm{d}V}. \tag{3.9}$$

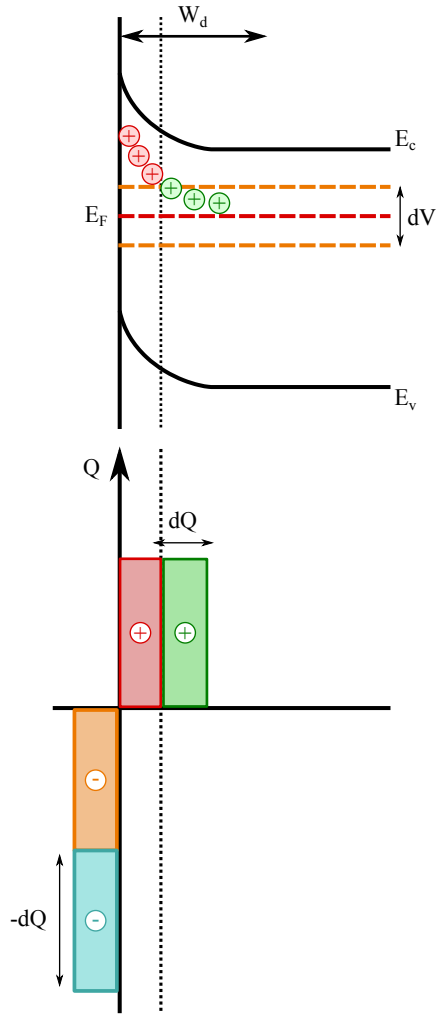


Figure 3.1: Depletion region and charge modulation of a Schottky diode in depletion ($C = dQ/dV$).

Integration of the doping concentration N_D, which is assumed to be uniform, over the depletion width W_d yields the total space charge $Q = N_D W_d A$, where A is the surface area of the junction. Differentiation of Eq. (3.8) with respect to V leads to

$$C = \frac{\mathrm{d}Q}{\mathrm{d}V} = A\sqrt{\frac{q\epsilon_r\epsilon_0 N_D}{2(V_d - V)}} \tag{3.10}$$

which is equivalent to the capacitance of a parallel plate capacitor of thick-

ness W_d and area A, with $C = \frac{\epsilon_r \epsilon_0 A}{W_d}$. The plot of $1/C^2$ as a function of V therefore yields a straight line, whose slope allows to obtain the doping concentration N_D. When the bias value V gets close to the built-in potential value V_d, the capacitance tends to increase towards infinity, as seen from Eq. (3.10), and the value of $1/C^2$ subsequently tends to zero. The x-intercept of such a $1/C^2$ plot therefore also corresponds to the built-in potential V_d as seen from the semiconductor.

If the doping concentration N_D is not uniform, this technique, then called C-V profiling [113], allows to probe the doping density as a function of depletion depth x_d into the semiconductor using the relations

$$N_D(x_d) = -\frac{2}{q\epsilon_r \epsilon_0 A^2 \frac{\partial(1/C^2)}{\partial V}} \tag{3.11}$$

$$x_d(C) = \frac{\epsilon_r \epsilon_0 A}{C} \tag{3.12}$$

The C-V technique is also routinely applied to pn junctions. In this case, however, the depletion capacitance depends on the carrier concentration on both side of the junction. The relation for the capacitance as a function of applied bias is

$$C = A\sqrt{\frac{q\epsilon_r \epsilon_0 N_A N_D}{2(V_d - V)(N_A + N_D)}}. \tag{3.13}$$

If either of the two sides of the junction is doped with a few orders of magnitude higher concentration, that is, e.g., if $N_A \gg N_D$, the previous relationship obtained from (3.10) between $1/C^2$ and N_D is recovered. Conversely, the p-doping concentration is obtained if $N_D \gg N_A$.

3.3 Principles of impedance spectroscopy

3.3.1 Impedance and complex formalism

The impedance of a semiconductor device is a measurement of the way it *impedes* the electrical current that might flow through it when a voltage is applied [114]. Let a sinusoidally oscillating potential of frequency $f = \omega/2\pi$,

$$v(t) = V\cos(\omega t) = \Re\left[\bar{V}e^{j\omega t}\right] = V\Re\left[e^{j\omega t}\right] \tag{3.14}$$

be applied across a semiconductor device. The resulting steady-state current is assumed to have the same frequency as the applied potential. This

hypothesis is only valid if the system is linear time-invariant (LTI), which implies a condition on the amplitude V that has to be relatively small (a few mV). However, the current may show a phase shift θ with respect to the potential and is therefore expressed as

$$i(t) = \Re\left[\bar{I}e^{j\omega t}\right] = I\cos(\omega t + \theta) = I\Re\left[e^{j\theta}e^{j\omega t}\right]. \tag{3.15}$$

In these equations, $\bar{V} = Ve^{j0}$ and $\bar{I} = Ie^{j\theta}$ are complex numbers called phasors, $V = \left|\bar{V}\right|$ and $I = \left|\bar{I}\right|$ are real numbers expressing the amplitude of the potential and current, respectively, $j^2 = -1$ and t is time. The phase of $\bar{V}$ is arbitrarily chosen as equal to zero, therefore acting as reference.

The impedance $\bar{Z}$ is expressed as a complex number, too, and is defined as the ratio of the applied potential $\bar{V}$ to the measured current $\bar{I}$,

$$\bar{Z}(\omega) = \frac{\bar{V}}{\bar{I}} = \frac{V}{I}e^{-j\theta} = Ze^{-j\theta}, \tag{3.16}$$

where $Z = \left|\bar{Z}\right|$ is the amplitude of the impedance $\bar{Z}(\omega) = \bar{V}/\bar{I}$, whose value depends on ω. The impedance therefore gives an account of both the relative amplitudes of the applied potential and resulting current, but also of the phase shift between the two, for a given frequency.

For actual measurements, it is necessary to measure the impedance during the application of various dc potentials. The potential $V(t)$ then takes the form

$$V(t) = V_0 + V\cos(\omega t) = V_0 + \Re\left[\bar{V}e^{j\omega t}\right] \tag{3.17}$$

where V_0 is a constant potential. That superimposed constant potential results in the combination of a constant, in phase component and an oscillating component to the measured current

$$I(t) = I_0 + I\cos(\omega t + \theta) = I_0 + \Re\left[\bar{I}e^{j\theta}e^{j\omega t}\right]. \tag{3.18}$$

3.3.2 Impedance, admittance and the complex plane

As a complex valued extension of the concept of resistance, the impedance can be expressed as the sum of a real and an imaginary part $\bar{Z} = \Re[\bar{Z}] + \Im[\bar{Z}] = R + jX$, where $R\,[\Omega]$ is simply called resistance and $X\,[\Omega]$ is the reactance.

The admittance $\bar{Y}$ is another quantity used to assess how easily a current can flow through a circuit. It is directly related to the impedance $\bar{Z}$ through

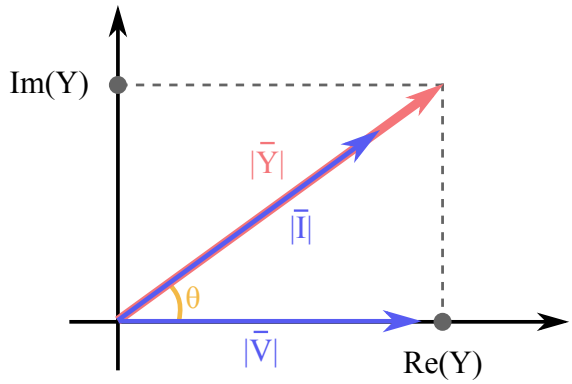


Figure 3.2: Phasors $\bar{V}$, $\bar{I}$ and admittance $\bar{Y}$ in the complex plane.

$\bar{Y} = \bar{Z}^{-1}$. The admittance $\bar{Y}$ can also be expressed as the sum of its real and imaginary parts $\bar{Y} = G + jB$, where $G\,[S]$ is the conductance and $B\,[S]$ is the susceptance. Transformation of parts of the impedance into admittance and vice-versa is performed through the following relationships:

$$G = \frac{R}{R^2 + X^2} \tag{3.19}$$

$$B = \frac{-X}{R^2 + X^2} \tag{3.20}$$

and conversely, the admittance can be transformed into impedance through

$$R = \frac{G}{G^2 + B^2} \tag{3.21}$$

$$X = \frac{-B}{G^2 + B^2} \tag{3.22}$$

The magnitude and direction of a planar vector such as the admittance $\bar{Y}$ can be expressed in a right-hand orthogonal system of axes by the vector sum of the components along the x and y axis, which relate to the real and imaginary parts of this vector. Using Euler's identity $e^{j\pi} = -1$, then $j = e^{j\pi/2}$ corresponds to an anticlockwise rotation by $\pi/2$, *i.e.* from the x-axis to the y-axis. The real part of Y is therefore represented in the direction of the real axis x and the imaginary part is plotted along the y axis. The sum vector can be plotted in the plane using either rectangular or polar coordinates, as shown in Fig. 3.2. Rectangular coordinates are expressed from the polar coordinates through

$$\begin{cases} x = \Re[\bar{Y}] & = \left|\bar{Y}\right| \cos\theta \\ y = \Im[\bar{Y}] & = \left|\bar{Y}\right| \sin\theta \end{cases} \tag{3.23}$$

while polar coordinates are obtained from the real and imaginary parts using the relationships:

$$\begin{cases} |\bar{Y}| & = \sqrt{\left(\Re[\bar{Y}]\right)^2 + \left(\Im[\bar{Y}]\right)^2} \\ \theta & = \arctan\left(\Im[\bar{Y}]/\Re[\bar{Y}]\right). \end{cases} \tag{3.24}$$

The admittance and impedance are time-invariant if the system it is applied to is also time-invariant. These quantities are generally *frequency-dependent*, though, and therefore denoted as $Y(\omega)$ and $Z(\omega)$. Usually, dependence on the applied dc bias V_0 and the temperature T is also observed. From the behaviour of $Y(\omega)$ or $Z(\omega)$ as a function of ω, electrical and material properties of semiconductor structures can be established, as will be discussed in the next Subsection.

The Kramers-Kronig relations apply to the connection between the real and imaginary parts of either the impedance or admittance [115, 116]. These relations therefore introduce some constraints between the real and imaginary parts. For instance, if $\Re[\bar{Y}]$ is found to be a function of frequency, then $\Im[\bar{Y}]$ cannot be zero over all frequencies, but has to vary with frequency, too. These constraints are very useful to assess the consistency of experimental impedance or admittance data.

3.3.3 Equivalent electrical circuit modeling

These real and imaginary parts of either the impedance or admittance can be conveniently considered as the elements of an equivalent electrical circuit, whose values depend on ω. A resistor can account for the real part of the impedance/admittance and a capacitor can support the role of the imaginary part. Impedances in series are simply added together to obtain the total equivalent impedance. The most straightforward way to model an arbitrary impedance is therefore to combine them in an RC series circuit, as shown in Fig. 3.3 (a). Parallel combinations are the easiest way to combine admittances, though, because the equivalent impedance of two parallel elements $Z_1 = 1/Y_1$ and $Z_2 = 1/Y_2$ is $Z_{//} = (1/Z_1 + 1/Z_2)^{-1} = (Y_1 + Y_2)^{-1} \Rightarrow Y_{//} = Z_{//}^{-1} = Y_1 + Y_2$. Admittances with arbitrary real and imaginary parts are therefore most readily represented by a parallel RC combination, as shown

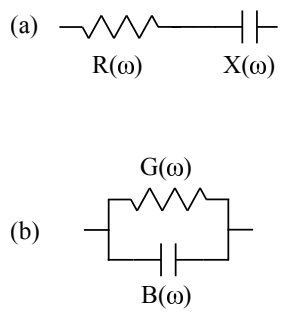


Figure 3.3: RC series - RC parallel schematics.

in Fig. 3.3 (b). Modeling the complete electrical response of a semiconductor device with an equivalent electrical circuit therefore consists in arranging various R and C elements in series or parallel combinations in order to account for the internal physical structure of the semiconductor device. This equivalent electrical model can subsequently be reduced to one of the basic circuits from Fig. 3.3 and its total impedance or admittance compared to the experimental data. Accurate modeling of the electrical properties of a semiconducting device requires that the total impedance or admittance of the model correspond to the experimental measurement, by fitting the values of the R, C elements from the model to the experimental data.

The difficulty, tough, resides in the fact that electrical circuits are not unique. Circuits containing more than three elements can indeed yield the same electrical response even though the elements are arranged in different ways. There is therefore no straightforward procedure to build an equivalent electrical circuit. One has to use intuition and physical justification of the elements brought into the modeled circuit and try to add as few elements as possible in order to keep the model simple.

The lumped-elements used in the models represent constant properties of the material leading to the complete, frequency dependent, impedance value. In some semiconductor devices, certain properties are distributed over a continuous range of energies or positions. The total impedance cannot consequently be correctly approximated by an equivalent electrical circuit unless one uses an infinite (or extremely large) distribution of lumped elements. Modeling based on microscopic parameters is usually a better approach for such cases.

3.3.4 Representation of admittance data

Admittance spectroscopy data can be represented in various ways, depending on the application. The first one consists in plotting both the so-called frequency-dependent capacitance, defined as $C(\omega) = B(\omega)/\omega$, and the conductance $G(\omega)$ over pulsation ω, $G(\omega)/\omega$, as a function of frequency f in a semilogarithmic scale. Such a representation of admittance data for an RC series electrical circuit containing frequency independent resistance $R_s = 100$ kΩ and capacitance $C_s = 1$ nF is shown in Fig. 3.4.

The peak in $G(\omega)/\omega$ as a function of frequency is related to the time constant τ of the RC circuit. This time constant is equal to $\tau = R_s C_s$ and the corresponding value of the frequency is

$$f_{\text{peak}} = \frac{1}{2\pi\tau}. \tag{3.25}$$

The capacitance curve shows a step corresponding to the peak of $G(\omega)/\omega$. For frequency going down to zero, $C(\omega)$ reaches a plateau, whose value is that of the frequency-independent capacitance C_s. The value of the peak of $G(\omega)/\omega$ is equal to $C_s/2$. These properties can be directly observed from the analytical expressions obtained by separating the real and imaginary parts of the admittance into

$$C(\omega) = \frac{C_s}{1 + \omega^2\tau^2} \tag{3.26}$$

$$G(\omega)/\omega = \frac{C_s\omega\tau}{1 + \omega^2\tau^2}. \tag{3.27}$$

Another way of representing the admittance data, widely used in electrochemistry [117], is the Nyquist plot [118, 119]. It consists in plotting the real and imaginary parts of the impedance Z in the complex plane. The angular frequency ω is the curvilinear coordinate, and each point of the graph corresponds to the impedance value at a given frequency. For a parallel RC circuit with resistance $R_p = 100$ kΩ and capacitance $C_p = 1$ nF, a semi-circle is obtained, as shown in Fig. 3.5. The radius of the semi-circle is related to the resistance value R_p. Frequency tends to infinity at the lowest resistance point and to zero at the highest resistance point, which is also equal to the value of R_p. In the Nyquist representation of an electrical circuit containing several elements, each RC couple is directly identified by an additional semi-circle in the complex plane. A drawback of this representation method is that the exact frequency of a given point is not directly available.

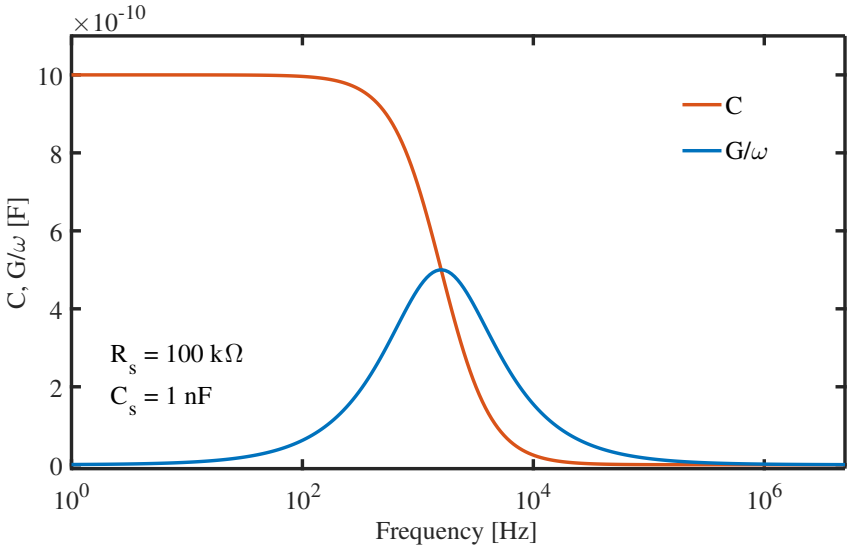


Figure 3.4: Admittance response of a RC series electrical circuit. Both $C(\omega)$ and $G(\omega)/\omega$ are plotted as a function of frequency.

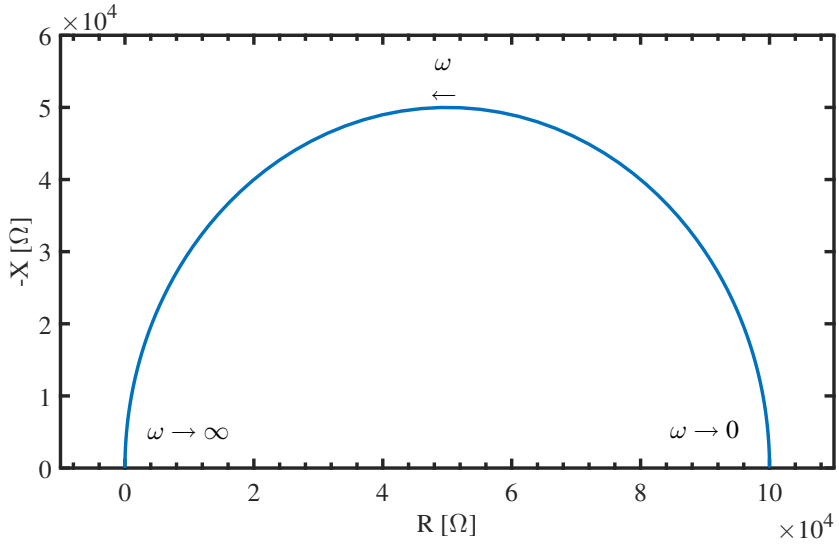


Figure 3.5: Nyquist plot of the impedance response of a RC parallel electrical circuit.

The basic RC series circuit model element is of particular importance because it is used to account for the presence of a defect level in semiconductor structures [120, 121, 122]. In the admittance data of a Schottky diode containing a defect level, for instance, a peak in the $G(\omega)/\omega$ curve and a step in $C(\omega)$ can be observed, whose position and height depend on the measurement temperature and dc bias applied to the diode. Modeling of the traps by an RC series circuit allows to simulate the trap time constant $\tau = RC$, which is related to physical parameters such as the emission coefficients.

The impedance behaviour of a plain Schottky diode can also be modeled by an equivalent electrical circuit, using a parallel R_dC_d circuit. The R_d element is the differential resistance of the diode and the capacitance element C_d accounts for the depletion capacitance [123, 120, 121].

Electrical circuit modeling then consists in fitting the values of the R and C elements to the experimental admittance data. The obtained values, that may vary with the applied dc bias and the temperature, provide a very useful insight into the physical processes that occur in the semiconducting structures.

3.4 MOS structures

Among the admittance methods for the characterization of interface traps, some based on C-V characteristics [124, 125] and others based on the conductance are found. C-V methods have the disadvantage that they require internal parameters such as the bias-dependent semiconductor capacitance to be known, or to be able to simulate ideal C-V characteristics as in the Terman method [126]. The conductance method, on the other hand, is very straightforward, with a direct link between the measurement and the interface trap density. The corresponding Fermi level position is also directly connected to the applied gate bias. The only parameter required is the oxide capacitance, which can be readily extracted from C-V measurements.

3.4.1 Ideal admittance behaviour of a MOS capacitor

In a MOS capacitor structure, four different regimes depending on the applied dc bias can be identified as well as their corresponding admittance behaviours. For a MOS structure with an n-type semiconductor, these are the

- **accumulation regime:** the applied bias is higher than the flatband potential, for which the bands are flat, *i.e.* constant over the whole

semiconductor material. This implies that the bands are bended in a way that leads to an accumulation of majority carriers at the MOS interface, as shown in Fig. 3.6 (a);

- **depletion regime:** the applied bias is such that the Fermi level is located below the flatband potential, near the intrinsic Fermi level, which means that the majority carriers are depleted and a space charge due to the ionized donors is formed;
- **weak inversion:** the Fermi level is now below the intrinsic Fermi level and above the threshold position, leading to the generation of a small density of minority carriers;
- **inversion**: the applied bias is lower than the threshold voltage and the density of minority carriers becomes larger than the doping density.

For p-type structures, relative bias values and Fermi level energies are reversed. Now, when the applied bias is *below* the flatband potential, accumulation occurs. Then when the applied bias is increased, the structure will go into the depletion regime, then the weak inversion and finally the strong inversion regime.

The ideal MOS capacitance can be derived from the description of the previous regimes. As it is assumed to be free of defects, the theoretical MOS capacitance is purely based on the free charges in the semiconductor and the metal separated by the dielectric oxide. The ideal MOS capacitance is represented by an oxide capacitance (C_{ox}) and a bias dependent semiconductor capacitance (C_s) in series [127], as depicted in Fig. 3.7. These capacitances account for the bias-dependent charge modulation over the oxide and the semiconductor, which is the small-signal capacitance $C = dQ/dV$.

Useful features can be extracted from the ideal MOS capacitance. The total capacitance is equal to the series combination of the oxide capacitance C_{ox} and semiconductor capacitance C_s

$$C = \frac{C_{ox}C_s}{C_{ox} + C_s}. \tag{3.28}$$

The semiconductor capacitance reaches its minimum value in accumulation, because in this regime, free charges accumulate towards the interface with the oxide, over only a very thin layer. As the oxide capacitance C_{ox} is considered to be constant, the total capacitance C therefore reaches its maximum value, and Eq. (3.28) tends to the oxide capacitance $C \approx C_{ox}$ if $C_s \ggg C_{ox}$. As the oxide capacitance is equal to

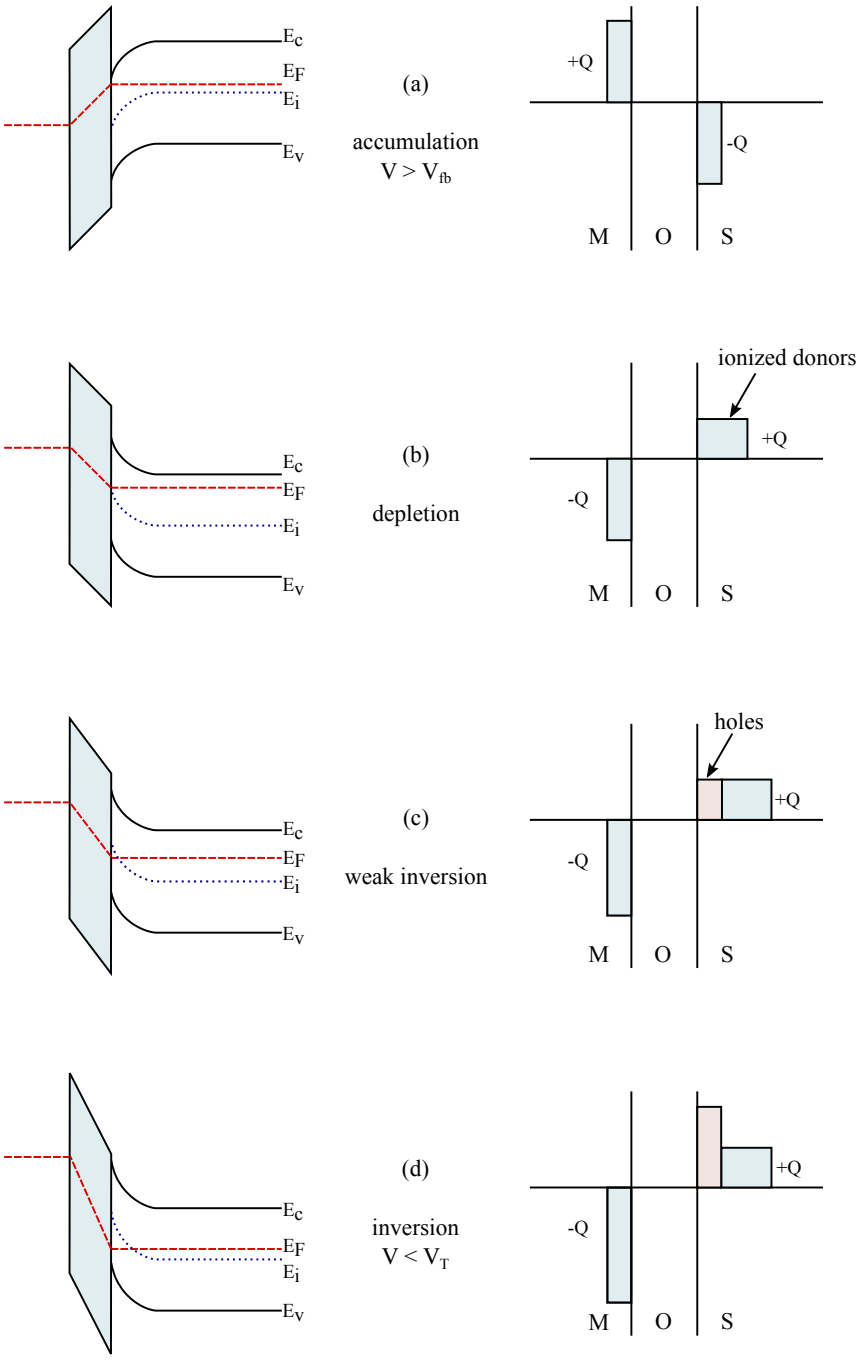


Figure 3.6: Schematic representation of the regimes of a MOS capacitor: accumulation (a), depletion (b), weak inversion (c) and strong inversion (c). Based on [111].

$$C_{ox} = \epsilon_{ox}/t_{ox}$$

where ϵ_{ox} is the dielectric constant of the oxide and t_{ox} is the thickness of the oxide. This can be used to extract the oxide thickness or EOT of MOS capacitors if ϵ_{ox} is known, or conversely to assess the value of ϵ_{ox} if the oxide thickness can be measured in another way.

The depletion capacitance C_s is related to the doping concentration through

$$C_s \approx \frac{\epsilon_s}{W_{\text{depletion}}} \approx \epsilon_s \sqrt{qN_D}$$

and the flatband potential V_{fb}, which is dependent on the fixed charge and the difference of the work functions between the semiconductor and the metal contact, can also be extracted from C-V measurements [127, 111].

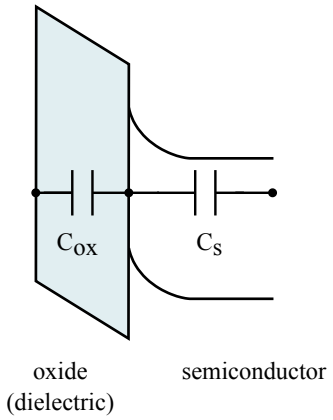


Figure 3.7: Ideal capacitance of a MOS structure, modeled as a series combination of an oxide capacitance C_{ox} and bias-dependent semiconductor capacitance C_s.

3.4.2 The conductance method

The conductance method is a characterization technique used to determine the density, capture probability and time constant dispersion of interface traps in MOS capacitor structures [128, 129, 130, 126]. It is based on the strong sensitivity of the admittance response to the presence of interface traps as compared to the admittance behaviour of an *ideal* MOS structure [131, 132, 133].

Interface traps are defects that are located at the interface between the semiconductor and the oxide and have energies comprised within the semiconductor bandgap. They can therefore exchange charges with either the conduction or valence band of this semiconductor by capturing or emitting electrons and holes. When the gate bias is changed, the Fermi level E_F at the interface of the semiconductor changes accordingly and traps located at energies close to E_F are either filled or emptied, depending on the relative move between E_F and the trap energy. As a small ac bias is applied to the gate, the Fermi level moves up and down, repeatingly modifying the trap occupancy. An energy loss will therefore occur because of the delay between the Fermi level change and the capture/emission of electrons by the trap. This energy loss is present at all frequencies, except the lowest frequencies where traps respond immediately (*i.e.* much faster than the ac frequency) to the change of E_F and the highest frequencies, where traps are not able to respond at all. This energy loss translates into a conductance (*i.e.* real part) component of the measured admittance .

Let us consider as an example an n-type semiconductor schematically represented in Fig. (3.8). During the first positive half-wave of the ac signal, the Fermi level at the interface moves closer to the conduction band and the average energy of the electrons in the conduction band will increase immediately (*i.e.*, much faster than the ac frequency). The traps, though, do not react immediately, because the exchange of charge between the trap and the valence or conduction band takes some time, that depends on the capture cross section of the trap and the energy difference with the bands [134] (see subsection 3.4.2.2 for a discussion on the traps time constant dependence). Empty interface traps at energies below the new Fermi level will therefore momentarily appear. When electrons from the conduction band are eventually captured by those traps, the captured electrons will have a higher average energy than the trap level. Those electrons will ultimately return to the energy level of the trap they are filling and the excess energy will dissipate in the semiconductor, through phonons heating up the lattice.

On the other negative half-wave of the ac signal, the Fermi level at the interface moves away from the conduction band and the electrons filling the traps that are above the new Fermi level will have an average energy higher than that of the other electrons in the semiconductor. When emission later occurs to restore those electrons to the conduction band, their excess energy also needs to dissipate into the lattice, inducing another energy loss.

There is therefore an energy loss on both half-cycles of the ac signal, which has to be supplied by the signal source, and translates into an equiv-

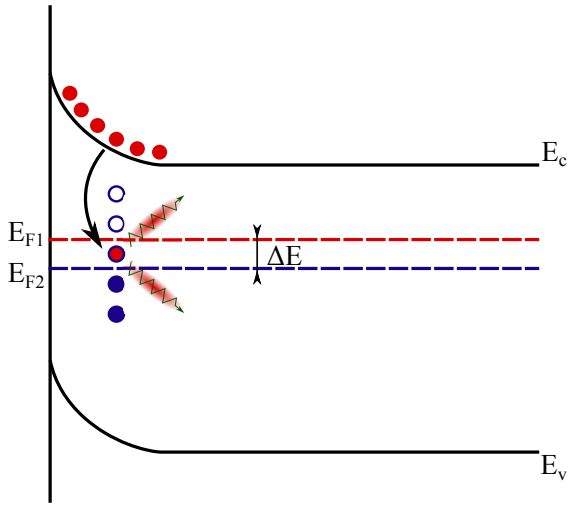


Figure 3.8: Energy loss during capture and emission of traps under ac bias.

alent conductance G_P that is parallel to the MOS capacitance and depends on the measurement frequency.

As interface traps retain electrons for some time after their capture, this also leads to the appearance of a small-signal capacitance $C_{it} = dQ/dV$ because of the variation of stored charges as a function of applied bias. The value of this capacitance signal is directly related to the interface trap density and is at the origin of the well-known "C-V bumps" observed in C-V measurements in the presence of interface traps.

For a given frequency of the ac signal, then, the energy loss will be dependent on both the density of interface traps and their capture probability, which is the speed at which they react. The full derivation of the expression of parallel conductance G_P is available in Ref. [127].

3.4.2.1 Interface trap density D_{it}

The important physical process to notice is that at very low frequency, the occupancy of the traps will change *in phase* with the ac signal because their time constant is much shorter than the period of the ac signal. No energy loss will occur and hence, the conductance G_P will be close to zero. As the frequency increases, traps will begin to lag behind the signal and energy loss will occur, leading to a measurable conductance G_P. This conductance will keep increasing until the ac signal will be so fast that traps will not have time to respond to the Fermi level change anymore. The conductance

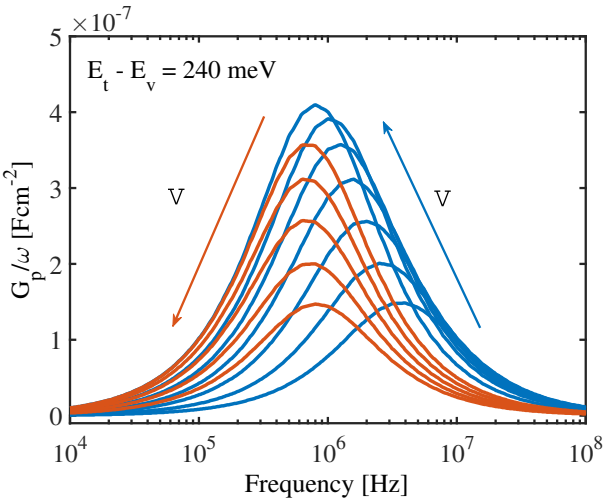


Figure 3.9: Conductance method: $(G_P/\omega)_{\max}$ as a function of frequency.

signal will therefore decrease until the traps do not respond at all anymore, and there is no measurable G_P, left. The frequency for which traps induce the maximum energy loss and conductance G_P is directly related to the interface trap density D_{it}. This D_{it} value is subsequently extracted from the relation [127]

$$D_{it} = \left(\frac{G_P}{\omega}\right)_{\max} [f_D(\sigma_s)q]^{-1}, \tag{3.29}$$

where $(G_P/\omega)_{\max}$ is the peak value of G_P/ω as a function of measurement frequency, for a given voltage. $f_D(\sigma_s)$ is a universal function of the surface potential fluctuation σ_s [127]. These potential fluctuations arise from the random *spatial* distribution of the discrete interface charges which induce a spatial distribution of band bendings at the oxide-semiconductor interface. The quantity σ_s therefore represents the standard deviation of these potential variations and the resulting asymmetry in the curve of G_P as a function of frequency. Values of $f_D(\sigma_s) = 0.4$ are theoretically predicted, although other slightly different, empirical values can be used to account for other effects such as the dispersion of time constants of the traps [135, 136, 137, 138].

In practical measurements, the parallel conductance G_P is obtained from the total measured admittance (G_m and C_m) by subtracting the oxide capacitance from the equivalent circuit model using relation [127]

$$\frac{G_P}{\omega} = \frac{\omega C_{ox}^2 G_m}{G_m^2 + \omega^2 \left(C_{ox} - C_m\right)^2}. \tag{3.30}$$

The extracted D_{it} value will correspond to the density of traps at an energy position in the semiconductor bandgap given by the Fermi level set by the applied steady state bias. This can be determined from the flatband potential, previously extracted from a C-V fit. One has to note that a large density of interface traps will slow down the displacement of the Fermi level with applied bias and reduce the accuracy of the resulting energy position. Numerical simulations of C-V characteristics including interface traps can be used to overcome such issues [139, 140], or relationships between the peak frequency at which G_P/ω is measured and energy position can be used (see Eq. (3.31) below).

The presence of a large series resistance can also influence the measurements, shifting the measured value of G_P by a constant. One can ensure that the series resistance is not too big by checking whether the conductance value scales with the area of the device measured, as the series resistance does not scale with it while interface trap density does.

3.4.2.2 Time constant and observable trap energies

As Eq. (3.31) shows, the interface trap time constant τ_{it} is particularly dependent on the energy position within the bandgap and on the temperature [127]

$$\tau_{it} = \left(v_{\text{th}}\, \sigma\, N_{\text{eff}}\, e^{(-q\Delta E/kT)}\right)^{-1}, \tag{3.31}$$

where v_{th} is the thermal velocity, σ is the capture cross section, N_{eff} is the effective density of states in the band holding the majority carriers and ΔE is the energy difference between the trap and the majority carrier band edge. The frequency range accessible to practical measurement equipment is limited and a trap can therefore be observed only if $(G_P/\omega)_{\text{max}}$ is within that range. This implies that only traps located in a limited part of the bandgap can be measured for a given temperature [141, 137, 142]. Figure 3.10 shows the observable energy ranges for Ge as a function of temperature and a frequency range of 1 kHz to 1 MHz. As the temperature is decreased, the interface traps frequency decreases as well, and the observable energy range moves towards the band edges. For high temperatures, traps located closer to midgap become accessible. Low bandgap materials such as Ge and GeSn

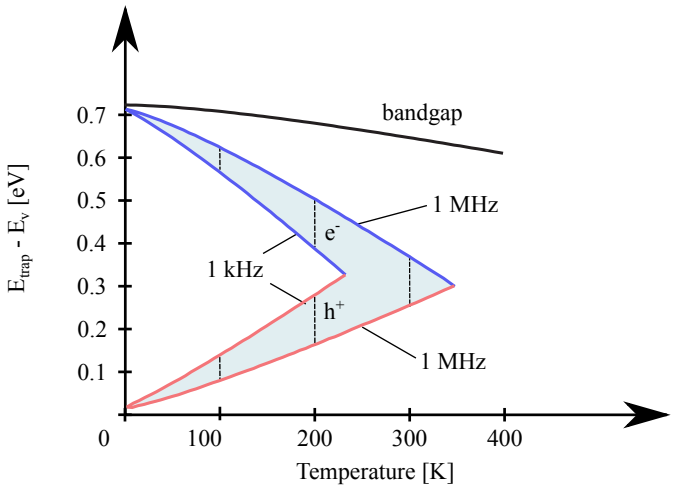


Figure 3.10: Observable energy range for Ge as a function of temperature for a given frequency window (1 kHz - 1 MHz) and an n-type (e^-) or p-type (h^+) semiconductor, from [141].

require a smaller temperature range in order to observe interface traps over the whole bandgap, as compared to larger bandgap materials such as GaAs.

3.4.2.3 Inversion response and impact on the extracted D_{it}

Many side effects can have an impact on the extracted D_{it} value and impair its accuracy. A major one, especially for small bandgap semiconductors, is the (weak) inversion response. The conductance method indeed assumes that the MOS structure is in depletion, meaning that the concentrations of both the majority and the minority carriers are at their minimum. When trying to probe interface traps beyond the depletion regime, weak inversion will begin to occur. The Fermi level is then such that the traps can communicate with both the conduction and the valence bands. Because of their small time constant, minority carriers filling the traps near the Fermi level can respond sufficiently fast and provide carriers to the minority band. The interaction of the traps with the majority carrier band will eventually result in an increased generation/recombination rate, mediated through the traps, and an increase in the observed conductance response. The extracted D_{it} value will therefore be overestimated. This effect is generally not observed in semiconductors such as Si because at practical frequencies, the inversion response is too weak to impact significantly the D_{it} value. For smaller bandgap semiconductors such as Ge and GeSn, though, minority carriers

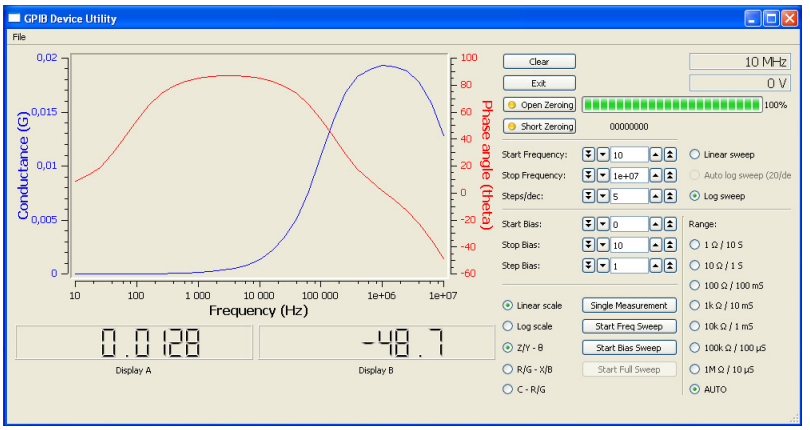


Figure 3.11: Home-made interface software performing an impedance measurement on the HP 4192A through GPIB.

are still able to interact with the traps in weak inversion in the frequency range 1 kHz - 1 MHz. This issue will be specifically addressed in Chapter 6, where the applicability of the conductance method to GeSn materials will be discussed.

A direct way to avoid this difficulty is to characterize both n-type and p-type semiconductors in order to probe each half of the bandgap in depletion, separately. This is not always possible, though, especially when the properties of the interface traps are dependent on the doping type of the semiconductor. Several other parameters can also have a strong impact on the results obtained from the conductance. Many of them are discussed in [127] and [141].

3.5 Experimental setup

An HP 4192A LF Impedance Analyzer, computer-controller through a GPIB interface, was used for most of the frequency measurements. These are performed with a home-made set of software interfaces tailored to allow various types of measurements (Fig. 3.11). The HP 4192A is able to sweep the frequency measurement from 5 Hz to 13 MHz, although that range was generally not used to its full extent in order to avoid both low and high frequency noises and coupling with other environmental sources. A practical frequency range used with typical probes and four terminal pair setup [143] is 100 Hz - 1 MHz. An ac bias oscillation with a 50 mV amplitude has usually been

Figure 3.12: Experimental setup for temperature-dependent measurements. The vertical position of the sample holder above the Dewar tank containing the liquid nitrogen controls the temperature.

applied, and it can be varied by 10 mV steps. An Agilent 4156 Semiconductor Parameter Analyzer was also used for some of the characterization. A Keithley 2400 Source Meter and a Keithley 2000 Multimeter were used in combination for I-V and time dependent measurements, through another set of home-made software interfaces.

3.5.1 Temperature-dependent measurements

Measurements as a function of temperature have been performed using a custom-made liquid nitrogen cryostat (Fig. 3.12). The temperature variation is based on positioning the sample holder above a Dewar bottle filled with liquid nitrogen, using an embedded electronic PID controller. The position of the sample holder in the vertical gradient of temperature between the temperature of liquid nitrogen (77 K) and room temperature allows to access a wide range of temperatures, as schematically depicted in Fig. 3.13.

The temperature is monitored through a high precision platinum resistor (Pt100) whose resistance is measured using a 24 Bits Analog/Digital

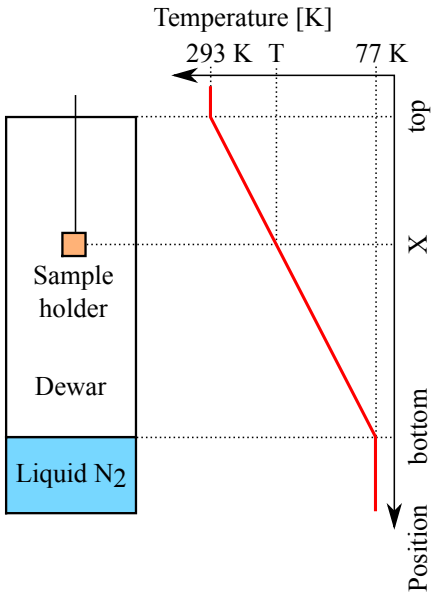


Figure 3.13: Schematic view of the custom-made liquid nitrogen cryostat and temperature dependence as a function of the sample holder position.

converter. The microcontroller then converts the resistance value into the actual temperature by looking up the closest resistance-temperature values in a table. The exact temperature is then obtained by interpolation between these data points. After stabilization, this setup is able to maintain the sample at the specified temperature with a precision of 0.1 K.

3.5.2 Sample holder

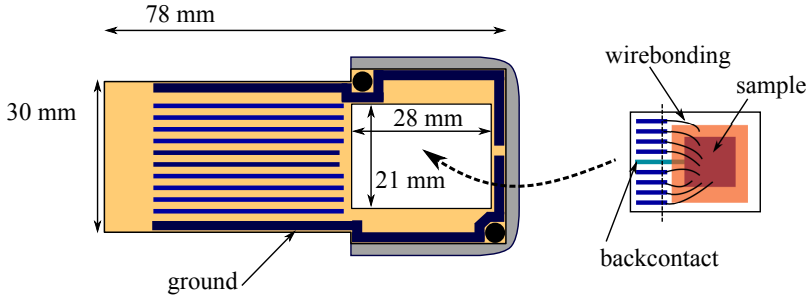


Figure 3.14: Schematic of the two parts of the sample holder.

The sample holder can receive bare, unpackaged pieces of wafers. They are glued with silver paste to a Copper square on a first PCB (right part of Fig. 3.14), which acts as backcontact. The top contacts are subsequently wirebonded from the sample to small tracks on the left of this small PCB. The small PCB is then placed on the larger sample holder (left of Fig. 3.14) where stronger wires are soldered between the small tracks on the PCB and the larger tracks on the sample holder. A maximum of eight top contacts and one backcontact tracks are available, which are extended with coaxial cables to allow an easy connection to the desired measurement equipment. A large ground track is also placed all around the sample holder, with a small slot in the middle to avoid loop interferences.

The aluminum casing of the sample holder is also fitted with the Pt100 resistor used to monitor the temperature, and four cables to allow the resistance measurement are connected to the holder as well. For temperature measurements, this sample holder is therefore seated in the cradle of the cryostat (Fig. 3.12) and tightly closed. All the cables are slipped into the vertical rod of the cryostat and then connected to the external equipment.

Chapter 4

Numerical simulations

In order to be able to analyze and simulate arbitrary semiconductor devices, a mathematical model has to be derived. The equations which form this model are commonly referred to as the *basic semiconductor equations* [144]. These equations account for the behaviour of semiconductors in a general way, without any particular assumptions. They are derived from Maxwell's equations and statistical relations from solid-state physics. Additional hypotheses are also introduced, though, such as the non-degeneracy of the semiconductor. These allow to obtain a set of equations that are not unnecessarily complex, so as to enable the numerical resolution of the problem while still covering a large range of cases.

In this Chapter, the basic semiconductor equations are established in Section 4.1: Poisson's equation, the continuity equations and transport equations. Then, the numerical procedure used for the solving of the system of equations is presented in Section 4.2, which is concluded by a discussion of the available solving algorithms.

4.1 The basic semiconductor equations

4.1.1 Poisson's equation

Poisson's equation expresses the relationship between a distribution of charges and the resulting electrical potential.

It is essentially a rewriting of Maxwell's equation

$$\nabla \cdot \mathbf{D} = \rho, \tag{4.1}$$

where ρ is the electric charge density and $\mathbf{D}$ is the electric displacement vector. This electric displacement vector $\mathbf{D}$ is linked to the electric field $\mathbf{E}$ through

$$\mathbf{D} = \epsilon \mathbf{E} \tag{4.2}$$

where ϵ is the permittivity of the material, provided that this permittivity is time independent. It is also a scalar value if the material under consideration is homogeneous and isotropic.

Introducing a vector potential $\mathbf{A}$, with $\nabla \cdot \mathbf{A} = 0$ and such that $\mathbf{B} = \nabla \times \mathbf{A}$, where $\mathbf{B}$ is the magnetic field, Maxwell's equation

$$\nabla \times \mathbf{E} = -\frac{\partial \mathbf{B}}{\partial t} \tag{4.3}$$

can be rewritten as

$$\nabla \times \left(\mathbf{E} + \frac{\partial \mathbf{A}}{\partial t} \right) = 0. \tag{4.4}$$

In vector analysis, if the curl of a vector field (in this case, $\mathbf{E} + \partial \mathbf{A}/\partial t$) is equal to zero, it can be expressed as a gradient field, *i.e.* $-\nabla \psi$. Using Eq. (4.2) to relate $\mathbf{E}$ and $\mathbf{D}$, we obtain

$$\mathbf{D} = -\epsilon \frac{\partial \mathbf{A}}{\partial t} - \epsilon \nabla \psi. \tag{4.5}$$

Inserted into the initial equation (4.1), this leads to

$$\nabla \cdot \left(\epsilon \frac{\partial \mathbf{A}}{\partial t} \right) + \nabla \cdot (\epsilon \nabla \psi) = -\rho. \tag{4.6}$$

Remembering that $\nabla \cdot \mathbf{A} = 0$ and that the permittivity ϵ is assumed to be homogeneous, the well-known form of the Poisson equation is finally obtained:

$$\epsilon \Delta \psi = -\rho \tag{4.7}$$

in which Δ stands for the Laplace operator $\Delta \psi = \nabla \cdot \nabla \psi$. The electric charge density can be broken down into the sum of the positively charged hole concentration p, ionized donor concentration N_D^+, the negatively charged electron concentration n, ionized acceptor concentration N_A^- and the charge related to the traps n_t^* times the elementary charge q:

$$\rho = q \left(p + N_D - n - N_A - n_t^* \right) \tag{4.8}$$

The quantity n_t^* represents the negative charge resulting from the trap concentration N_t and is expressed as

$$\text{with } n_t^* = \begin{cases} n_t & \text{if } N_t \text{ is acceptor-type} \\ -(N_t - n_t) & \text{if } N_t \text{ is donor-type.} \end{cases}$$

The breaking down of ρ in Eq. 4.8 doesn't add any new assumptions to those made to obtain Poisson's equation, as it is only a mathematical substitution. The subsequent modeling of the quantities represented by p, n, N_D^+, N_A^- and n_t^* will make use of statistical relations from solid-state physics, though.

4.1.2 Continuity equations

The divergence operator is applied to Maxwell's equation for the magnetic field $\mathbf{H}$:

$$\nabla \cdot (\nabla \times \mathbf{H}) = \nabla \cdot \left(\mathbf{J} + \frac{\partial \mathbf{D}}{\partial t} \right) \tag{4.9}$$

where $\mathbf{J}$ is the current density. Considering that the application of the divergence operator to the curl of a vector field is equal to zero ($\nabla \cdot (\nabla \times \mathbf{A}) = 0$), we obtain

$$\nabla \cdot \mathbf{J} + \frac{\partial \rho}{\partial t} = 0. \tag{4.10}$$

The total current density $\mathbf{J}$ can be broken down into the sum of a component $\mathbf{J}_n$ accounting for the current caused by electrons and a component $\mathbf{J}_p$ accounting for the current caused by holes. By expanding the expression of ρ into its constituents (see Eq. (4.8)) in Eq. (4.10), it can be rewritten as

$$\nabla \cdot (\mathbf{J}_n + \mathbf{J}_p) + q \frac{\partial \left(p + N_D - n - N_A - n_t^* \right)}{\partial t} = 0. \tag{4.11}$$

The physical interpretation of this relation is that sources and sinks of the total conduction current $\mathbf{J}$ are entirely compensated by the time variation of the charge density. Defining the *displacement current* $\mathbf{J}_D \equiv \partial \mathbf{D} / \partial t$, Eq. (4.11) can also be written as

$$\nabla \cdot (\mathbf{J}_n + \mathbf{J}_p + \mathbf{J}_D) = 0 \tag{4.12}$$

showing that the sum of all current components is a non-divergent vector field. This implies that in 1-dimensional situations, $\mathbf{J}_n + \mathbf{J}_p + \mathbf{J}_D$ is independent of the spatial coordinate x.

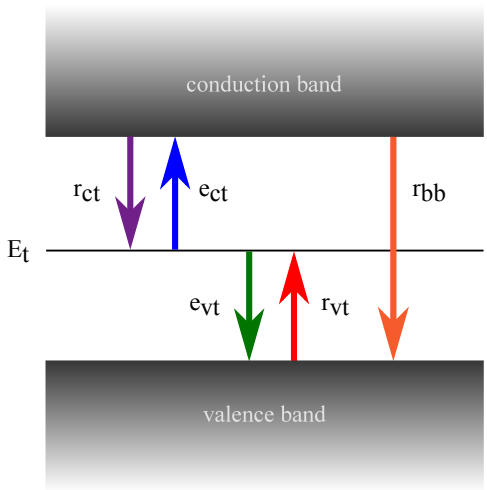


Figure 4.1: Microscopic transition rates: r_{ct} and e_{ct} for the conduction band recombination and emission from the trap level, e_{vt} and r_{vt} for the emission and recombination with the valence band and r_{bb} for band-to-band radiative recombinations.

Assuming that the ionization of donor and acceptor dopants is time-independent, Eq. (4.11) can be rewritten as

$$\nabla \cdot \mathbf{J}_n - q\frac{\partial n}{\partial t} + \nabla \cdot \mathbf{J}_p + q\frac{\partial p}{\partial t} - q\frac{\partial n_t^*}{\partial t} = 0. \tag{4.13}$$

Two recombinations terms R_n and R_p are then introduced and Eq. (4.13) can be further decomposed into three parts:

$$\nabla \cdot \mathbf{J}_n - q\frac{\partial n}{\partial t} = qR_n \tag{4.14}$$

$$\nabla \cdot \mathbf{J}_p + q\frac{\partial p}{\partial t} = -qR_p \tag{4.15}$$

$$-q\frac{\partial n_t^*}{\partial t} = -q\left(R_n - R_p\right). \tag{4.16}$$

Splitting up Eq. (4.13) does not provide new information. However, these terms contribute to a meaningful interpretation of the variation of charge carrier concentration. The quantities R_n and R_p, expressed in $[m^{-3}s^{-1}]$, can be understood as representing exchanges between the electrons, holes and traps. R_n accounts for the net recombination or generation of electrons and

a positive value indicates recombinations ($\partial n/\partial t < 0$), whereas a negative value indicates generation of electrons. Similarly, R_p stands for the net recombination or generation of holes.

These quantities R_n and R_p then need to be *modelled* in order to account for the actual behaviour of semiconducting structures. Electrons and holes emission and capture rates by traps have to be included, as well as radiative transitions. Other examples of physical processes that lead to generation or recombination are Auger effects, impact ionization or optical excitation by light. Optical excitation is also implemented in the software as an optional parameter and is discussed below.

Carriers recombination with traps

Trap levels can capture or emit electrons and holes, modifying their charge state. The recombination and generation mechanisms have been characterized by Shockley, Read and Hall, whose initials were given to these types of traps. The probability for a SRH trap to capture an electron from the conduction band is proportional to the carrier density n and to the unoccupied trap concentration $N_t - n_t$. A capture coefficient for electrons, c_n, is defined and expressed as the product of the capture cross section for electrons σ_n and the electron thermal velocity v_n^{th}. The recombination rate for electrons, expressed in $[m^{-3}s^{-1}]$, is therefore

$$r_{ct} = c_n\, n\,(N_t - n_t) = \sigma_n\, v_n^{th}\, n\,(N_t - n_t)\,. \tag{4.17}$$

The thermal velocity of electrons, defined by Maxwell and Boltzmann's kinetic theory of gases, is expressed by

$$v_n^{th} = \sqrt{\frac{3kT}{m_e}}.$$

Electrons can also be emitted from the trap state to the conduction band, at a rate e_{ct} that is proportional to the density of occupied traps

$$e_{ct} = e_n\, n_t$$

where e_n is the thermal emission rate. The net recombination rate of electrons from the conduction band to the trap level r_n is finally expressed as the difference of the previous two rates:

$$r_n = r_{ct} - e_{ct} = c_n\, n(N_t - n_t) - e_n n_t \tag{4.18}$$

Capture and emission transitions of holes with the valence band can be described in a similar way. The net recombination rate of holes from the valence band to the trap state is given by

$$r_p = r_{vt} - e_{vt}$$

where r_{vt} and e_{ct} are the recombination and emission rates of electrons from the valence band, respectively. They are expressed as

$$r_{vt} = c_p\, p\, n_t \tag{4.19}$$
$$e_{vt} = e_p(N_t - n_t). \tag{4.20}$$

Again, c_p is expressed from the hole thermal velocity v_p^{th} and the hole capture cross section σ_p as

$$c_p = \sigma_p v_p^{th}.$$

Radiative recombinations

Regarding radiative transitions, the probability of electron-hole recombination is proportional to $np - n_i^2$, where n_i is the intrinsic carrier concentration. Indeed, the product of the electron and hole concentrations at equilibrium is a constant $np = n_i^2$. If those quantities depart from equilibrium because of the application of an external stimulus, recombinations or generations will increase proportionally to $np - n_i^2$, in order to bring the concentrations back to equilibrium. If extra carriers have been generated, recombinations will increase and if carriers have been removed, generations will prevail, until a steady state equilibrium situation between generation/recombination and the external excitation is reached. The band-to-band radiative recombination term is

$$r_{bb} = B_r \left(np - n_i^2\right) \tag{4.21}$$

where B_r is the semiconductor radiative recombination constant $\left[m^3 s^{-1}\right]$.

The net generation/recombination terms can then be written as

$$R_n = r_n + r_{bb} \tag{4.22}$$
$$R_p = r_p + r_{bb}. \tag{4.23}$$

Figure 4.1 schematically depicts these capture and emission processes.

Optical generation

Optical generation of electrons and holes from traps can also be included by the addition of two terms to the previous relations for R_n and R_p: the optical electron generation rate $g_n[m^{-3}s^{-1}]$ and the optical hole generation rate g_p. The probability to emit an electron from the trap level because of optical excitation is proportional to the occupancy of that trap and to the incident flux of photons $\Phi[m^{-2}s^{-1}]$

$$g_n = \sigma_n^o \Phi n_t \tag{4.24}$$

where σ_n^o is the electron optical capture cross section $[m^2]$, representative of the probability that an incoming photon transfer its energy to an electron occupying the trap level. The optical hole generation can be defined in the same way as

$$g_p = \sigma_p^o \Phi \left(N_t - n_t\right) \tag{4.25}$$

where σ_p^o is the hole optical capture cross section.

4.1.3 Transport equations

The derivation of the current relations for the $\mathbf{J}_n$ and $\mathbf{J}_p$ components from the Boltzmann Transport Equations (BTE) is very lengthy and complex. Their comprehensive establishment encompasses a very large field of physics that goes far beyond the goal of this work. Therefore only the main steps of the development used to obtain the final results will be described below, in order to highlight the physical basis and hypotheses that support the final relations. Complete developments can be found, for instance, in [145, 146].

The current components $\mathbf{J}_p$ and $\mathbf{J}_n$ can be written, without loss of generality, as

$$\mathbf{J}_p = qp\mathbf{v}_p \tag{4.26}$$

$$\mathbf{J}_n = -qn\mathbf{v}_n \tag{4.27}$$

where $\mathbf{v}_p$ and $\mathbf{v}_n$ are the average velocities of the holes and electrons, respectively.

To obtain information on those velocities, the carrier concentration is described by means of a function f_p for holes (f_n for electrons) in the phase

space, containing all spatial coordinates $\mathbf{x} = (x, y, z)$, momentum coordinates $\mathbf{k} = (k_x, k_y, k_z)$ and time t. The carrier concentration is therefore given by f_p (or f_n) per unit volume of the phase space, which in this case has seven dimensions. With the proper normalization, f_p (f_n) can therefore also be seen as the probability to find a certain carrier type in a given phase space coordinate [147].

Boltzmann's equation [148] written for a given carrier type i (which can stand for either n or p) states that

$$\frac{\partial f_i}{\partial t} = \left(\frac{\partial f_i}{\partial t}\right)_{\text{force}} + \left(\frac{\partial f_i}{\partial t}\right)_{\text{diff}} + \left(\frac{\partial f_i}{\partial t}\right)_{\text{coll}} \tag{4.28}$$

where the *force* term is related to the external forces $\mathbf{F}_t$ exerted on the carriers. In our case it solely consists of the electric field $\mathbf{E}$, as the impact of the magnetic induction $\mathbf{B}$ will not considered. The *diff* term represents the diffusion of the carriers and *coll* is the "collision" or scattering term, taking into account all the internal properties and processes such as impurity atoms or ions, vacancies or thermal lattice vibrations. To establish the so-called *drift-diffusion* equations first developed by Van Roosbroeck [149], we expand the Boltzmann equation (4.28) into

$$\frac{\partial f_i}{\partial t} = -\frac{\mathbf{F}_t}{\hbar} \cdot \nabla_k f_i(\mathbf{x}, \mathbf{k}) - \mathbf{v} \cdot \nabla_x f_i(\mathbf{x}, \mathbf{k}) + \left.\frac{\partial f_i}{\partial t}\right|_{\text{coll}} \tag{4.29}$$

where $\nabla_k f_i(\mathbf{x}, \mathbf{k})$ denotes the gradient of $f_i(\mathbf{x}, \mathbf{k})$ with respect to the momentum coordinates $\mathbf{k}$ and $\nabla_x f_i(\mathbf{x}, \mathbf{k})$ is the gradient of $f_i(\mathbf{x}, \mathbf{k})$ with respect to the spatial coordinates $\mathbf{x}$. The collision term $\left.\frac{\partial f_i}{\partial t}\right|_{\text{coll}}$ refers to a myriad of internal processes that cannot be calculated explicitly. It is therefore expressed as the product of a scattering rate $S(\mathbf{k}, \mathbf{k}')$ from state $\mathbf{k}$ to $\mathbf{k}'$ and the distribution function f_i

$$\left.\frac{\partial f_i(\mathbf{k})}{\partial t}\right|_{\text{coll}} = \sum_{\mathbf{k}'} \left[S(\mathbf{k}', \mathbf{k}) f_i(\mathbf{k}') \left[1 - f_i(\mathbf{k})\right] - S(\mathbf{k}, \mathbf{k}') f_i(\mathbf{k}) \left[1 - f_i(\mathbf{k}')\right]\right]. \tag{4.30}$$

The first term in the sum describes the number of carriers scattered from a different state $\mathbf{k}'$ into the state $\mathbf{k}$, $f_i(\mathbf{k}')$ being the probability that such a different state is occupied and $[1 - f_i(\mathbf{k})]$ the probability that the state $\mathbf{k}$ is unoccupied and is therefore available. The second term correspondingly describes the number of carrier being scattered from a state $\mathbf{k}$ into a different state $\mathbf{k}'$. More details on the scattering probability $S(\mathbf{k}, \mathbf{k}')$ can be found

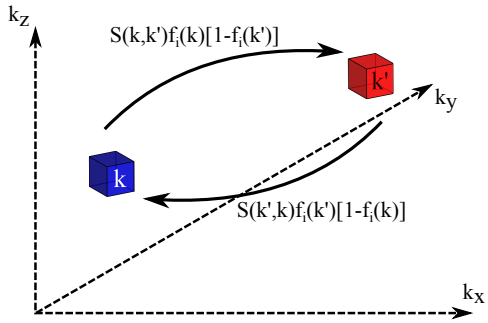


Figure 4.2: The scattering rate from state $\mathbf{k}$ to state $\mathbf{k}'$ is equal to the product of $f_i(\mathbf{k})$, the occupation probability of state $\mathbf{k}$, $[1 - f_i(\mathbf{k}')]$, the probability that state $\mathbf{k}'$ is unoccupied and the scattering probability from state $\mathbf{k}$ to state $\mathbf{k}'$, $S(\mathbf{k}, \mathbf{k}')$. Conversely, the scattering rate from state $\mathbf{k}'$ to state $\mathbf{k}$ is $S(\mathbf{k}', \mathbf{k}) f_i(\mathbf{k}')[1 - f_i(\mathbf{k})]$.

in ref. [150, 151]. In the case of elastic scattering, $S(\mathbf{k}, \mathbf{k}') = S(\mathbf{k}', \mathbf{k})$ and $\left.\frac{\partial f_i}{\partial t}\right|_{coll}$ reduces to

$$\left.\frac{\partial f_i(\mathbf{k})}{\partial t}\right|_{coll} = \sum_{\mathbf{k}'} S(\mathbf{k}, \mathbf{k}') \left[f_i(\mathbf{k}') - f_i(\mathbf{k})\right] \tag{4.31}$$

If it is now assumed that the external forces $\mathbf{F}_t$ and gradients have been applied for a very long time, they have driven the distribution function from its equilibrium value $f_{i,0}$ to a steady state value f_i. If this deviation from equilibrium is small, the following relation can be assumed to hold:

$$\frac{\partial f_i}{\partial t} = \left.\frac{\partial f_i}{\partial t}\right|_{coll} = -\frac{f_i - f_{i,0}}{\tau_i} \tag{4.32}$$

where τ_i is the relaxation time of either holes or electrons, characterizing the rate of return to the equilibrium state from the disturbed state. This assumption is known as the *relaxation time* approximation [149], allowing to obtain a solution to the Boltzmann transport equation, which now rewrites as

$$\frac{\partial f_i}{\partial t} = -\frac{\mathbf{F}_t}{\hbar} \cdot \nabla_k f_i(\mathbf{k}) - \mathbf{v} \cdot \nabla_x f_i(\mathbf{k}) - \frac{f_i - f_{i,0}}{\tau_i} \tag{4.33}$$

Multiplying Eq. (4.33) by the group velocity $\mathbf{v}$, integrating over the entire moment space $\mathbf{k}$ and further assuming that the external forces $\mathbf{F}_t$ can

be expressed as $\mathbf{F}_t = q\mathbf{E}$ (for holes) or $\mathbf{F}_t = -q\mathbf{E}$ (for electrons), ordinary differential equations for the drift velocities of holes and electrons are obtained [152, 150, 153]

$$\frac{\partial}{\partial t}\left(p\mathbf{v}_p\right) - \frac{q}{m_p^*}\, p\,\mathbf{E} + \frac{1}{m_p^*}\nabla\left(pkT\right) = -\frac{p\mathbf{v}_p}{\tau_p} \tag{4.34}$$

$$\frac{\partial}{\partial t}\left(n\mathbf{v}_n\right) + \frac{q}{m_n^*}\, n\,\mathbf{E} + \frac{1}{m_n^*}\nabla\left(nkT\right) = -\frac{n\mathbf{v}_n}{\tau_n} \tag{4.35}$$

Introducing the effective carrier mobilities μ_p and μ_n

$$\mu_p = \frac{q\tau_p}{m_p^*},\ \mu_n = \frac{q\tau_n}{m_n^*} \tag{4.36}$$

where m_p^* and m_n^* are the hole and electron effective mass, respectively, and given the form of the current equations (4.26) and (4.27), Eq. (4.34) and (4.35) rewrite as

$$\tau_p\frac{\partial \mathbf{J}_p}{\partial t} + \mathbf{J}_p = q\mu_p p\left(\mathbf{E} - \frac{1}{p}\nabla\left(p\frac{kT}{q}\right)\right) \tag{4.37}$$

$$\tau_n\frac{\partial \mathbf{J}_n}{\partial t} + \mathbf{J}_n = q\mu_n p\left(\mathbf{E} + \frac{1}{n}\nabla\left(n\frac{kT}{q}\right)\right) \tag{4.38}$$

The relaxation times τ_p and τ_n are very small, typically of the order of 10^{-12} s or below, which suggest to regard Eqs. (4.37) and (4.38) as singularly perturbed, expand their solution into powers of the perturbation parameter and take the zeroth order term to obtain the current densities

$$\mathbf{J}_{p0} = q\mu_p p\left(\mathbf{E} - \frac{1}{p}\nabla\left(p\frac{kT}{q}\right)\right) \tag{4.39}$$

$$\mathbf{J}_{n0} = q\mu_n n\left(\mathbf{E} + \frac{1}{n}\nabla\left(n\frac{kT}{q}\right)\right) \tag{4.40}$$

which are therefore approximations of order τ_p (or τ_n). Under the hypothesis that the lattice temperature T is constant and using substitutions known as the Einstein relations to define the holes and electrons diffusion constants,

$$D_p = \mu_p\frac{kT}{q} \tag{4.41}$$

$$D_n = \mu_n\frac{kT}{q} \tag{4.42}$$

the final form of the current relations can be written as the sum of a drift and a diffusion component

$$\mathbf{J}_p \cong qp\mu_p\mathbf{E} - qD_p\nabla p \tag{4.43}$$

$$\mathbf{J}_n \cong qn\mu_n\mathbf{E} + qD_n\nabla n. \tag{4.44}$$

The final relations are valid, provided that a certain number of assumptions are made. Among them, the most significant ones which are related to our uses are:

- all scattering processes are elastic so that, e.g., optical phonon scattering is neglected;
- effects of degeneracy have been neglected, so that only non-degenerate semiconductors should be considered;
- the carrier temperature is assumed to be constant and equal to that of the lattice, so that hot-carriers cannot be considered, either;
- parabolic energy bands are assumed, which is another reason why degenerate semiconductors should not be considered;
- the semiconductor is assumed to be infinitely large, so the drift-diffusion approximation is expected to fail within a few mean free paths from the boundaries such as contacts or interfaces [154, 155]. For the numerical solution of the system, boundary conditions will need to be set anyway, so that the issue will first lie on the accurate modelling of those boundary values.

$$\nabla \cdot (\epsilon_s \nabla \psi) = q\,(p + N_D - n - N_A - n_t^*) \tag{4.45}$$

$$\frac{\partial n}{\partial t} = \frac{1}{q}\nabla \cdot \mathbf{J}_n - c_n n\,(N_t - n_t) + e_n n_t + B_r\left(np - n_i^2\right) \tag{4.46}$$

$$\frac{\partial p}{\partial t} = -\frac{1}{q}\nabla \cdot \mathbf{J}_p - c_p p n_t + e_n\,(N_t - n_t) + B_r\left(np - n_i^2\right) \tag{4.47}$$

$$\frac{\partial n_t}{\partial t} = c_n n\,(N_t - n_t) - e_n n_t - c_p p n_t + e_n\,(N_t - n_t) \tag{4.48}$$

$$\mathbf{J}_n = qn\mu_n \mathbf{E} + qD_n \nabla n \tag{4.49}$$

$$\mathbf{J}_p = qp\mu_p \mathbf{E} - qD_p \nabla p \tag{4.50}$$

Figure 4.3: The basic semiconductor equations

4.2 Numerical resolution

The semiconductor equations from Fig. (4.3) will form the basis of the numerical model to be solved. Substituting Eq. (4.49) and (4.50) into Eq. (4.46) and (4.47) along with Poisson's equation (4.45) leads to four coupled, non-linear partial differential equations with the four dependent variables ψ, n, p and n_t. In order to obtain a numerical solution, the corresponding problem will have to be set on a given geometry with boundary conditions. All dependent variables will be scaled appropriately and the geometry will be discretized in order to obtain a non-linear algebraic system that has approximately the same behaviour as the continuous system. The non-linear system is then solved by linearization and iterative refinement of the solution, starting from an initial guess value. The iterative procedure is repeated until the corrections are small enough to expect the numerical solution to be close to the mathematical solution or when it is clear that convergence towards the desired solution will not occur.

In the choice of iterative or direct solution methods for the non-linear system, attention will be directed to the convergence, accuracy, robustness and efficiency of the method. The convergence will determine whether a solution is reached, accuracy will define how close to the mathematical solution the numerical solution will be. Robustness is the ability to converge to the solution even when the initial guess is far from the solution, or using

meshes with coarser precisions. Finally, the efficiency is a measure of how fast the solution will be obtained.

In practical situations, all semiconductor structures are three-dimensional. However, the devices under consideration are often fundamentally two- or even one-dimensional objects. This implies that many devices can be modelled along only one dimension: the partial derivatives of the parameters and dependent variables of the basic semiconductor equations perpendicular to a line are zero, which simplifies greatly the calculations.

4.2.1 Dependent variables and physical parameters

The directly obvious dependent variables that appear in the basic semiconductor equations are ψ, n, p and n_t. Another set of variables that can be used is (ψ, F_n, F_p, F_t) [156, 157, 158], which is related to the previous set (ψ, n, p, n_t) through the Boltzmann approximation for the carrier concentrations in non-degenerate semiconductors and the Fermi-Dirac statistics for the trap state,

$$n = N_c \, \mathrm{e}^{-\frac{E_c - F_n}{kT}} \tag{4.51}$$

$$p = N_v \, \mathrm{e}^{-\frac{F_p - E_v}{kT}} \tag{4.52}$$

$$n_t = \frac{N_t}{1 + g_t \mathrm{e}^{\frac{E_t - F_t}{kT}}} \tag{4.53}$$

where N_c, N_v are the effective density of states in the conduction and the valence band, respectively, N_t is the total concentration of the trap state and F_n, F_p and F_t are the quasi-Fermi energies for electrons, holes and electrons on occupied trap level, respectively. This substitution is nothing more than a mathematical change of variables, which is advantageous because all variables in the set (ψ, F_n, F_p, F_t) now have the same order of magnitude. Another benefit of this set is that all carrier concentrations are now perforce positive, as opposed to the lowly negative values that may arise from numerical errors in the (ψ, n, p, n_t) variables set [144].

4.2.2 Meshing, scaling and discretization

The equations subsequently have to be scaled, in order to improve the numerical behaviour of the following resolution steps. All parameters and variables are replaced by their scaled values and the basic equations are also

Quantity	Scaling factor	Value
Position	x_0	10^{-6} m
Mobility	μ_0	1 $\mathrm{cm^2V^{-1}s^{-1}}$
Electric potential	ψ_0	kT/q
Concentration	N_0	$1/x_0^3$
Electric field	E_0	ψ_0/x_0
Diffusion constant	D_0	μ_0/x_0
Velocity	v_0	D_0/x_0
Current density	J_0	qN_0D_0/x_0
Recombination	R_0	D_0N_0/x_0^2
Time	τ_0	N_0/R_0

Table 4.1: Scaling scheme for the dependent variables and physical parameters.

scaled accordingly to the new variable scales. Many scaling schemes can be envisioned [159, 160, 161, 162]: the scaling that has been used in the current work is based on these, with some empirical alterations to ensure a proper numerical conditioning of the solution, namely a fixed value of $x_0 = 10^{-6}$ m. The complete scaling scheme used is given in Table 4.1.

The geometry of the problem to be solved then needs to be discretized: the spatial domain is partitioned into a finite number of subdomains in which the solution will be calculated with a desired accuracy. The differential equations are subsequently approximated in each of the subdomains by algebraic equations that depend on values of the dependent variables evaluated only at discrete points in the domain. This generates a usually large system of non-linear equations whose unknowns are the value of the dependent variables at discrete points, that has to be solved using linearization techniques detailed later in this chapter.

Using this method, an exact solution of the initial analytical formulation of the problem is impossible to obtain: only an exact solution of the discretized non-linear algebraic equations can be reached. The quality of the approximation of the solution will therefore depend directly upon the

spatial resolution of the subdomains defined in the discretization scheme.

The approach used here is called the finite-difference method (FDM) because it approximates the differential equations by difference equations involving only the nearest points of the discretized domains. Another method, the finite elements method (FEM), approximates the *solution* of the system instead of the equations over a given subdomain. Both methods are very similar to each other from a mathematical point of view and although finite elements methods are now widely used in many fields, finite difference methods remain a strong contender because of their relatively easy and intuitive formulation [163].

Geometrical discretization of the domain, also called *meshing*, therefore involves defining points where the dependent variables will take well-defined values. Increasing the number of such points obviously increases the accuracy of the approximation, although at the cost of a proportionally increasing computational effort. A trade-off therefore has to be found between the requirements of accuracy, which requires a fine mesh, and numerical efficiency. The ideal size of the mesh is especially difficult to determine, as the quality of the solution is not known at this stage yet.

Meshes are generally not uniform, which makes it possible to refine the mesh around regions of particular interest or where the unknowns show strong variations.

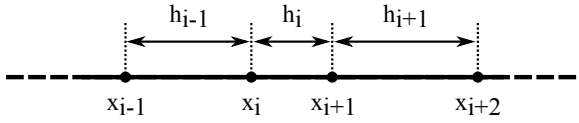


Figure 4.4: Meshing in one dimension

The distance between two successive points x_i and x_{i+1} is defined as h_i, as depicted in Fig. 4.4, where the i subscripts indicate the value of the quantity at mesh point index i on the grid, that is

$$h_i = x_{i+1} - x_i \tag{4.54}$$

Poisson's equation is discretized in a fairly straightforward manner, using a three point difference scheme that yields an approximation to the order $\mathcal{O}(h)$ in one dimension. In the case of spatial variation of the relative dielectric constant ϵ_{rs}, care must be taken as to which value of ϵ to use at each discretization point. The scaled Poisson equation is

$$\lambda_0^2 \frac{\partial}{\partial x}\left(\frac{\partial \psi}{\partial x}\right) = (n - p + N_A - N_D - n_t^*) \tag{4.55}$$

where x is the spatial coordinate and λ_0 is the Debye screening length that appears as a result of the chosen scaling parameters

$$\lambda_0 = \sqrt{\frac{\epsilon_0 \epsilon_{rs} kT}{q^2 N_0 x_0^2}} \tag{4.56}$$

Typical values of λ_0 found in practical situations are in the range of 10^{-11}. All variables and parameters in Eq. (4.55) are scaled, although the same notations are used for simplicity. Replacing the first order partial derivatives with finite differences

$$\left.\frac{\partial \psi}{\partial x}\right|_i = \frac{\psi_{i+1/2} - \psi_{i-1/2}}{\frac{h_i + h_{i-1}}{2}} \tag{4.57}$$

into Eq. (4.55) gives

$$\lambda_0^2 \left(\frac{\left.\frac{\partial \psi}{\partial x}\right|_{i+1/2} - \left.\frac{\partial \psi}{\partial x}\right|_{i-1/2}}{\frac{h_i + h_{i-1}}{2}} \right) - n_i + p_i - N_A + N_D + n_{t,i}^* = 0. \tag{4.58}$$

The derivatives at mid-interval values of ψ are then again replaced with difference approximations, assuming that the variation of ψ are linear ($\partial\psi/\partial x$ is constant)

$$\left.\frac{\partial \psi}{\partial x}\right|_{i+1/2} = \frac{\psi_{i+1} - \psi_i}{h_i} \tag{4.59}$$

which finally leads to

$$\lambda_0^2 \left(\frac{\frac{\psi_{i+1} - \psi_i}{h_i} - \frac{\psi_i - \psi_{i-1}}{h_{i-1}}}{\frac{h_i + h_{i-1}}{2}} \right) - n_i + p_i - N_A + N_D + n_{t,i}^* = 0 \tag{4.60}$$

In order to be able to consider a relative dielectric constant whose value is dependent on the position, a second-order derivative using a three points discretization has to be used, including ϵ_{rs} in the first derivative in $\lambda_0^2 \frac{\partial}{\partial x}\left(\epsilon_{rs} \frac{\partial \psi}{\partial x}\right)$, which gives rise to the following coefficients for the terms ψ_i, ψ_{i-1}, ψ_{i+1} :

$$\begin{aligned} a_{i-1} &= \epsilon_{i-1}\frac{h_i^2}{h_{i-1}^2\left(h_{i-1}+h_i\right)^2}+\epsilon_i\frac{3h_{i-1}-h_i}{h_{i-1}^2\left(h_{i-1}+h_i\right)} \\ &\quad -\epsilon_{i+1}\frac{1}{\left(h_{i-1}+h_i\right)^2} \qquad (4.61) \\ a_i &= \epsilon_{i-1}\frac{h_i-h_{i-1}}{h_{i-1}^2\left(h_{i-1}+h_i\right)}+\epsilon_i\frac{\left(h_i-h_{i-1}\right)^2-2h_{i-1}h_i}{h_{i-1}^2h_i^2} \\ &\quad -\epsilon_{i+1}\frac{h_i-h_{i-1}}{h_i^2\left(h_{i-1}+h_i\right)} \qquad (4.62) \\ a_{i+1} &= \epsilon_{i-1}\frac{-1}{\left(h_{i-1}+h_i\right)^2}+\epsilon_i\frac{3h_i-h_{i-1}}{h_i^2\left(h_{i-1}+h_i\right)}-\epsilon_{i+1}\frac{h_{i-1}^2}{h_i^2\left(h_{i-1}+h_i\right)} \qquad (4.63) \end{aligned}$$

in Poisson's equation

$$\lambda_0^2\left(a_{i-1}\psi_{i-1}+a_i\psi_i+a_{i+1}\psi_{i+1}\right)-n_i+p_i-N_A+N_D+n_{t,i}^*=0 \qquad (4.64)$$

Discretization of the continuity equations under steady-state conditions is a bit more involved, as large exponential variations of the carrier concentrations are present. These variations can range over several orders of magnitude and linear interpolation is therefore not adequate. Scharfetter and Gummel have first suggested to assume instead that the current densities J_n, J_p and the electric field $\partial\psi/\partial x$ are constant over each discretization interval, which proved to be more reliable [164, 165]. This means that the electrical potential is linearly interpolated between each mesh point.

In order to avoid any confusion, one should note that all subsequent equations are written in terms of the scaled variables and parameters, albeit notations similar to the unscaled ones are used to save from unnecessary heaviness.

The scaled current equations are therefore

$$\begin{aligned} J_n &= -\mu_n n\frac{\partial\psi}{\partial x}+D_n\frac{\partial n}{\partial x} \qquad (4.65) \\ J_p &= -\mu_p p\frac{\partial\psi}{\partial x}-D_n\frac{\partial p}{\partial x}. \qquad (4.66) \end{aligned}$$

As a result of the scaling, it is immediately obvious that

$$\frac{D_n}{\mu_n}=\frac{D_p}{\mu_p}=1 \qquad (4.67)$$

so that Eq. (4.65) and (4.66) rewrite as

$$\frac{\partial n}{\partial x} = n\frac{\partial \psi}{\partial x} + \frac{J_n}{\mu_n} \tag{4.68}$$

$$\frac{\partial p}{\partial x} = -p\frac{\partial \psi}{\partial x} - \frac{J_p}{\mu_p}. \tag{4.69}$$

Under the previously made assumption that J_n and $E = -\partial\psi/\partial x$ are constant over the interval $x \in [x_i,\, x_{i+1}]$, Eq. (4.68) for the electrons is a first order differential equation whose solution is

$$n\left(x \in [x_i,\, x_{i+1}]\right) = Ce^{-Ex} + \frac{J_n}{\mu_n E} \tag{4.70}$$

where C is a constant whose value will be determined by the boundary condition. This boundary condition is $n(x_i) = n_i$, which leads to

$$n\left(x \in [x_i,\, x_{i+1}]\right) = n_i e^{E(x_i - x)} + \frac{J_n}{\mu_n E}\left(1 - e^{E(x_i - x)}\right) \tag{4.71}$$

Taking the value of Eq. (4.71) for x_{i+1}, $n(x_{i+1}) = n_{i+1}$, rearranging to obtain the value of J_n and substituting E by $-\left(\psi_{i+1} - \psi_i\right)/h_i$ results in

$$J_n = \frac{\mu_n}{h_i}\left(\frac{-Eh_i}{e^{-Eh_i} - 1}n_{i+1} - \frac{Eh_i}{e^{Eh_i} - 1}n_i\right) \tag{4.72}$$

$$= \frac{\mu_n}{h_i}\left[\frac{\psi_{i+1} - \psi_i}{e^{\left(\psi_{i+1} - \psi_i\right)} - 1}n_{i+1} - \frac{\psi_i - \psi_{i+1}}{e^{\left(\psi_i - \psi_{i+1}\right)} - 1}n_i\right] \tag{4.73}$$

$$= \frac{\mu_n}{h_i}\left[B\left(\psi_{i+1} - \psi_i\right)n_{i+1} - B\left(\psi_i - \psi_{i+1}\right)n_i\right] \tag{4.74}$$

where $B(x)$ is the Bernoulli function, defined as

$$B(x) = \frac{x}{e^x - 1}. \tag{4.75}$$

This function, which is plotted in Figure 4.5, is not defined for $x = 0$, although the limit for $x \to 0$ is 1. Particular attention will therefore need to be paid to avoid truncation errors during the numerical evaluation of this function.

The discretization of the continuity equation for electrons can now be performed, under steady-state conditions (*i.e.* $\partial/\partial t = 0$). The discretized stationary continuity equation for electrons is

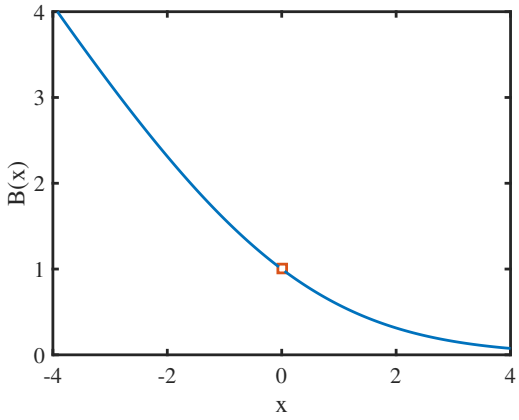


Figure 4.5: The Bernoulli function $B(x)$.

$$\frac{J_n|_{i+1/2} - J_n|_{i-1/2}}{\frac{h_i + h_{i-1}}{2}} - R_n = 0 \tag{4.76}$$

and as J_n is assumed to be constant over the interval $[x_i, x_{i+1}]$, then $J_n|_{i+1/2}$, the value at $x = (x_i + x_{i+1})/2$ is also equal to J_n and the continuity equation for electrons at point index i reads

$$\begin{aligned} &\frac{2\,\mu_n|_{i+1/2}}{h_i\,(h_i + h_{i-1})}\left[B\left(\psi_{i+1} - \psi_i\right) n_{i+1} - B\left(\psi_i - \psi_{i+1}\right) n_i\right] \\ -&\frac{2\,\mu_n|_{i-1/2}}{h_{i-1}\,(h_i + h_{i-1})}\left[B\left(\psi_i - \psi_{i-1}\right) n_i - B\left(\psi_{i-1} - \psi_i\right) n_{i-1}\right] \\ &- R_n|_i \;=\; 0 \end{aligned} \tag{4.77}$$

The discretized continuity equation for holes is obtained through the same developments and is

$$\begin{aligned} &\frac{2\,\mu_p|_{i+1/2}}{h_i\,(h_i + h_{i-1})}\left[B\left(\psi_{i+1} - \psi_i\right) p_i - B\left(\psi_i - \psi_{i+1}\right) p_{i+1}\right] \\ -&\frac{2\,\mu_p|_{i-1/2}}{h_{i-1}\,(h_i + h_{i-1})}\left[B\left(\psi_i - \psi_{i-1}\right) p_{i-1} - B\left(\psi_{i-1} - \psi_i\right) p_i\right] \\ &- R_p|_i \;=\; 0 \end{aligned} \tag{4.78}$$

The steady-state trap continuity equation is easily discretized. Its depends only on the local values, yielding the following relation

$$R_n|_i - R_p|_i = 0 \tag{4.79}$$

4.2.3 Boundary conditions

The previous relations for the discretization of the semiconductor equations are valid for all inner points of the mesh. In order to obtain a well-posed problem, adequate boundary conditions need to be set. Boundary conditions for the electric potential ψ and the quasi-Fermi levels for n, p and n_t are necessary. In the case of low current densities or low contact resistance, the Fermi levels are usually assumed to take their equilibrium values at the contacts [166]. Therefore F_n, F_p and F_t are all equal at the contact, assuming infinite surface recombination velocities, which is usually done. However, if the contacts are not far enough, *i.e.* at least a few diffusion lengths away from regions where the carrier concentrations and electric field vary strongly, the Fermi levels have not yet recovered their equilibrium values. Finite surface recombination velocities subsequently have to be considered and some intermediate value of the Fermi level is obtained as a result [144].

In this framework, though, thermal equilibrium at the contacts will be assumed, so that all Fermi levels are equal and their position relative to the band edges can be calculated by enforcing local charge neutrality at the boundary. In the absence of external bias, the built-in potential V_{bi} is the relative shift of the band edges between the left contact, with coordinate x_L and the right contact x_R. If an external bias V_{ext} is applied to the semiconductor, it will appear directly at the contacts. Considering the potential at the left boundary as the reference, the boundary conditions for the electric potential of an ohmic contact are

$$\psi(x_L) = 0 \text{ and } \psi(x_R) = V_{bi} + V_{ext} \tag{4.80}$$

Schottky contacts can also be considered. The physics of Schottky contacts is extremely complex, though, and a highly simplified model will be used for the purpose of simulation. The result will be the direct shift of the electric potential at the Schottky contact by the equivalent of the barrier height ϕ_s [167]

$$\psi(x_L) = 0 \text{ and } \psi(x_R) = V_{bi} + V_{ext} + \phi_s \tag{4.81}$$

For the boundary conditions of the Fermi levels, the relations are

$$F_n(x_L) = F_p(x_L) = F_t(x_L) = 0 \tag{4.82}$$

$$F_n(x_R) = F_p(x_R) = F_t(x_R) = -V_{ext} \tag{4.83}$$

For non-ideal contacts, a phenomenological model consisting in the combination of a thermionic and a diffusion is to be used [168, 169]. The carrier concentrations at the contacts are then related to the current densities through the carrier surface recombination velocities for electrons v_n and holes v_p

$$J_n = -qv_n\,(n - n_0) \tag{4.84}$$

$$J_p = qv_p\,(p - p_0) \tag{4.85}$$

From the values of the carrier concentrations, boundary conditions for the corresponding Fermi levels can be calculated. These conditions reduce to Eqs. (4.82) and (4.83) only if the boundary is far enough from the injection region, so that n and p have returned to their equilibrium values. The rate of return to equilibrium is exponential with a decay length that is equal to the minority-carrier diffusion length. Charge neutrality will therefore be almost established after a few decay lengths, even though a larger distance will be necessary for the Fermi levels to reach equilibrium, as their rate of change is only $1\,kT$ per diffusion length and they can be initially separated from equilibrium by tens of kT [166].

4.2.4 Linearization and solving algorithms

The non-linear system of equations resulting from the discretization on the mesh now has to be solved. For this, the dependent variables in the entire geometric domain are filled with initial values, forming a guess solution. These values are based on the boundary conditions, for instance by basic linear interpolation or stepsize increments between the different values of the boundary conditions. The system of equations is then linearized and iteratively solved. The initial guess is successively updated through corrections provided by the solution of the linearized systems. The iterations continue until a convergence criteria is reached, or until a fixed number of iterations has been performed without reaching the convergence criteria, which indicates that the solution will probably never be reached under these conditions. In this case, the solution can be reached by trying a different initial guess, using a more refined mesh, or using another iteration technique.

Among the algorithms that can be used for solving these non-linear systems are the Newton method and the Gummel method [144]. In the Newton iteration method, a linearized version of the entire non-linear system is solved at each step. The size of this system can be quite large and can therefore take a long time to compute if the mesh contains many points. Reaching convergence should require a limited number of iterations if the initial guess is sufficiently close to the solution, though. The Newton-Richardson method is a modified version of the Newton method that calculates a new version of the linearized system of equations only when the rate of convergence is seen to decrease below a certain threshold. In order to avoid a phenomenon known as *overshoot*, which describe a tendency of Newton methods to overestimate the correction steps, a limitation of the size of the correction applied at each step can be implemented [170]. The convergence rate of Newton methods is quadratic, so that if the convergence requires a large number of iterations with any of these Newton methods, the problem is most likely poorly conditioned [171]. Possible reasons are: the mesh may be too coarse, the initial guess may be too far from the solution, or assumptions necessary to the correct formulation of the problem may not be encountered as expected, e.g. depletion regions extending into a region defined as an Ohmic contact.

In Gummel's method, on the other hand, only one equation is linearized and solved at a time. That equation is linearized with respect to its primary dependent variable, and all other variables are kept at their most recently computed values, thus providing a correction to that primary dependent variable only. Another equation is then linearized and solved in the same manner, until all dependent variables have been updated to their new value. The process is repeated until a convergence criteria is reached, as in the Newton method. The Gummel method usually accommodates a poor initial guess, but frequently shows a rate of convergence that is lower than that of Newton method. Newton methods also being generally more efficient for strongly coupled equations, as are the semiconductor equations, a modified Newton-Richardson method has been used in this work.

The linearization procedure for the Newton method is introduced below [172], for the case of steady-state conditions. The four discretized equations are written for each point of the meshed geometry, which can be summarized by the vector function $\mathbf{f}$:

$$\begin{cases} f_1\left(\{\psi, F_n, F_p, F_t\}\right) &= 0 \\ f_2\left(\{\psi, F_n, F_p, F_t\}\right) &= 0 \\ f_3\left(\{\psi, F_n, F_p, F_t\}\right) &= 0 \\ f_4\left(\{\psi, F_n, F_p, F_t\}\right) &= 0 \end{cases} \tag{4.86}$$

where f_1, f_2, f_3 and f_4 are the Poisson's equation, electron, holes and trap continuity equations, respectively. The set $\{\psi, F_n, F_p, F_t\}$ is made of the $4N$ elements of the solution vector $\mathbf{w}$ that contains the values of the variables at all mesh points, with N the total number of mesh points. The condensed writing of Eq. (4.86) can be expressed as follows:

$$\mathbf{f}(\mathbf{w}) = 0 \tag{4.87}$$

If $\mathbf{w}^k$ is the solution estimate at iteration k, then

$$\mathbf{f}(\mathbf{w}^k) = 0 \tag{4.88}$$

and defining $\delta\mathbf{w}^k = \mathbf{w}^{k+1} - \mathbf{w}^k$ the correction to be applied to reach the next step, the Taylor expansion limited to the first order of the equations around the solution $\mathbf{w}^k$ gives

$$\mathbf{f}(\mathbf{w}^{k+1}) = \mathbf{f}(\mathbf{w}^k) + \nabla_{\mathbf{w}}\, f|_{\mathbf{w}=\mathbf{w}^k}\, \delta\mathbf{w}^k \tag{4.89}$$

where $\mathrm{J} = \nabla_{\mathbf{w}}\, f|_{\mathbf{w}=\mathbf{w}^k}$ is the Jacobian matrix of the system of equations computed at iteration k. The order of the error resulting from the first truncated term in the Taylor expansion is $\mathcal{O}\left(\left[\delta\mathbf{w}^k\right]^2\right)$. The solution at the next iteration must satisfy the equation system, so that

$$\mathbf{f}(\mathbf{w}^{k+1}) = 0 \tag{4.90}$$

and therefore

$$\mathrm{J}\,\delta\mathbf{w}^k = -\mathbf{f}(\mathbf{w}^k) \tag{4.91}$$

The unknown vector correction $\delta\mathbf{w}^k$ is then determined by solving the linear system given by Eq. (4.91). The Jacobian matrix J is obtained through the computation of the derivatives of the semiconductor equations with respect to the dependent variables. This is done using the following relations

$$\delta n = n(\delta\psi + \delta F_n) \tag{4.92}$$
$$\delta p = p(\delta\psi + \delta F_p) \tag{4.93}$$
$$\delta n_t = n_t\beta(\delta\psi + \delta F_t) \tag{4.94}$$

with

$$\beta = \frac{g_t e^{E_t - F_t}}{1 + g_t e^{E_t - F_t}} \tag{4.95}$$

The correction steps $\delta\mathbf{w}^k$ are multiplied by a damping factor α before being applied to the solution $\mathbf{w}^{k+1}$ in order to avoid overshoot of the solution. Values of $\alpha = 0.5$ are generally used, but can be even lower when trying to overcome difficult convergence in some situations.

Small-signal analysis

The preceding discretization and solving developments have been performed under steady-state conditions. Another regime of great interest is the small-signal analysis, where the externally applied voltage contains a sinusoidally oscillating component of frequency f and amplitude $\tilde{V}$ in addition to the steady-state value V_0. This is the regime of impedance spectroscopy and capacitance voltage characterizations. The amplitude of $\tilde{V}$ has to be small with respect to kT/q for the small-signal conditions to be valid. In this regime, all variables have a steady-state value, denoted by an index 0 and obtained by the numerical resolution procedure that is detailed above. There is also a sinusoidal, harmonic, component with a complex amplitude [173], denoted by the adjunction of a tilde to the said value:

$$\psi(x,t) = \psi_0(x) + \tilde{\psi}(x)e^{j\omega t} \tag{4.96}$$
$$p(x,t) = \mathrm{p}_0(x) + \tilde{p}(x)e^{j\omega t} \tag{4.97}$$
$$n(x,t) = \mathrm{n}_0(x) + \tilde{n}(x)e^{j\omega t} \tag{4.98}$$
$$n_t(x,t) = \mathrm{n}_{t,0}(x) + \tilde{n}_t(x)e^{j\omega t} \tag{4.99}$$

The semiconductor equations can then be rewritten in terms of the corresponding small-signal quantities, as shown in Fig. 4.6.

$$\nabla \cdot \left(\epsilon_s \nabla \tilde{\psi}\right) = -q\left(\tilde{p} - \tilde{n} - \tilde{n}_t^*\right) \tag{4.100}$$

$$j\omega\tilde{n} = \frac{1}{q}\nabla \cdot \tilde{\mathbf{J}}_n - \tilde{R}_{bb} + \tilde{R}_{nt} \tag{4.101}$$

$$j\omega\tilde{p} = -\frac{1}{q}\nabla \cdot \tilde{\mathbf{J}}_p - \tilde{R}_{bb} - \tilde{R}_{pt} \tag{4.102}$$

$$j\omega\tilde{n}_t = \tilde{R}_{nt} - \tilde{R}_{pt} \tag{4.103}$$

Figure 4.6: The basic semiconductor equations in the small-signal regime.

As their form is entirely similar to the equations for the steady-state regime, the same numerical procedure is used. The values of the small-signal carrier concentrations are obtained using the steady-state values and a first order approximation by

$$\tilde{n} = n_0\left(q\tilde{\psi} + \tilde{F}_n\right)/kT \tag{4.104}$$

$$\tilde{p} = -p_0\left(q\tilde{\psi} + \tilde{F}_p\right)/kT \tag{4.105}$$

$$\tilde{n}_t = n_{t,0}\left(q\tilde{\psi} + \tilde{F}_t\right)/kT \tag{4.106}$$

The boundary conditions for the potential $\tilde{\psi}$ and quasi-Fermi levels $\tilde{F}_n$, $\tilde{F}_p$ and $\tilde{F}_t$ are now simply equal to the amplitude of the small-signal potential $\tilde{V}$. Detailed developments can be found in Refs. [174, 175, 176, 139, 144].

Solving algorithms for the linear systems

Repeated solving of linear systems of equations is a necessary process for the iterative methods described above. Either direct or iterative (indirect) solving algorithms can be used, the first being able to solve the system of equation in a known number of operations and the second after a number of iterations that depends on the convergence of an initial guess towards the solution. Direct methods therefore produce solutions that are exact within the numerical roundoff and truncation limits, whereas iterative methods give a solution that is within the set convergence criteria.

The size of the problem to be solved depends on the number $m = 4$ of unknowns for a given mesh point and the total number of mesh points N. The total number of unknowns is therefore obviously $m \times N$. The coefficient

matrix to be used in the case of Newton's method contains $(m \times N)^2$ elements, while each iteration of a unique equation in Gummel's method would have led to a coefficient matrix with just N^2 elements. There is therefore a trade-off to be made between a large number of mesh points, which increases the quality and precision of the solution, and the resulting huge linear system to be solved. Current computers typically have more than enough memory capacity to store linear systems with a few thousand points, which is a comfortable number to simulate typical device applications. Another hurdle encountered in the processing of large linear systems is that when the entire matrix cannot be stored in the CPU memory cache, the computational performance is drastically reduced. With the ever-increasing size of the CPU cache, though, this is also less and less of a problem.

In addition, the linear systems that have to be solved have the property that their coefficient matrices are generally sparse, meaning that they contain many zero elements. Informed ordering of the mesh points therefore allow to obtain matrices that are diagonal, tri-diagonal or more generally banded matrices (matrices where only elements a few columns away from the diagonal are non-zero). If the coefficient matrix is not oversized, direct methods taking this particular structure into account for optimization are generally used, as is done in this work. Iterative methods, which use less memory and do not suffer as much from the performance drop when exceeding the memory cache size, will have to be used for very large problems which cannot be conveniently solved using direct methods.

Chapter 5

GeSn based pn junctions

Parts of this chapter have been published in the following articles :

- **Baert, B.**, Gupta, S., Gencarelli, F., Loo, R., Simoen, E., & Nguyen, N. D. (2015). Electrical characterization of p-GeSn/n-Ge diodes with interface traps under dc and ac regimes. *Solid-State Electronics*, **110**, 65-70. http://hdl.handle.net/2268/178856
- **Baert, B.**, Nakatsuka, O., Zaima, S., & Nguyen, N. D. (2013). Impedance Spectroscopy of GeSn-based Heterostructures. *ECS Transactions*, **50**(9), 481-490. http://hdl.handle.net/2268/127051

The many attractive properties of the GeSn semiconducting alloy make it a very interesting material for various applications. Its direct bandgap and increased carrier mobilities, as already discussed in Chapter 2, cause a strong interest in using it for next generation complementary metal oxide semiconductor (CMOS) devices. Because of the lattice mismatch with Ge or Si, it can be used as stressor or strained material. It is therefore, for instance, a good candidate as compressive source and drain stressor in p-type Ge-channel metal oxide semiconductor field effect transistors (pMOSFETs) [177, 178, 179, 180]. It is also expected to be able to play a role as channel material [181, 182] within a postscaling approach [13]. On the road to obtain these high performing GeSn devices, diodes are useful tools to investigate the material properties of GeSn layers. The process flow for diodes indeed contains much of the steps necessary for the fabrication of a full MOSFET device. Thin GeSn layers will be required for the envisioned applications, and pn diodes allow to study the origins of the leakage current and evaluate in particular the consequences of defects at the GeSn/Ge interface.

In Section 5.1, simulation of GeSn based materials is introduced along with a discussion of the specific numerical difficulties associated with these materials. The electrical characteristics of Boron doped p-GeSn/n-Ge diodes are analyzed in Section 5.3. Both room-temperature and temperature dependent measurements are used, notably to investigate the reverse current of the diodes. Simulations of analogous semiconducting structures are used to probe the effect of traps at the GeSn/Ge interface and show that the presence of a trap level ~ 200 meV above the valence band is best able to replicate the experimental current measurements. The impact of those traps on the overall C-V characteristics, however, is also shown to be relatively limited, as indicated by the assessment of the frequency dependence and Mott-Schottky analysis of the diodes characteristics performed in Subsection 5.3.2.

Section 5.4 then discusses electrical measurements of unpassivated mesa p-GeSn/n-Ge diodes. Very long transients are observed during the measurement of the current over time for a fixed reverse bias. Dipping the diodes in H_2O_2 completely removes these transients, which are therefore clearly associated with the presence of native oxide on the unpassivated diode sidewalls. Various dependences of the transients are explored, especially in view of establishing conditions that would allow to perform repeatable measurements or obtain measurements similar to those acquired from temporarily H_2O_2 passivated diodes. Finally, an electrical model involving RC branches with

a distribution of time constants to account for the conduction through the sidewalls is presented. Fitting to the experimental data shows the need for very large time constants to obtain currents similar to those of passivated diodes.

5.1 Theoretical investigation and simulations

Theoretical simulations performed on a test device first allow to evaluate the general characteristics of GeSn based diodes. These initial simulations provide a first insight into the behaviour of the electrical parameters of GeSn materials. The numerical obstacles that can potentially occur while running the solving algorithms under these specific conditions can also be assessed. The main numerical difficulty in these simulations results from the small bandgap energy of Ge and GeSn materials. The Fermi level easily moves across the whole bandgap, leading to huge spatial variations that impair the convergence of the solution. Because of these small bandgaps, the Fermi level can even move beyond the band edges, thus invalidating the assumption made in the development of the numerical method that the semiconductor is non-degenerate. Such a situation can already happen when applying small external biases and therefore appropriate caution must be considered when interpreting results obtained from the numerical simulations. The high mobility values involved in the materials under consideration also decrease the well-conditioning of the Jacobian matrices in the solving algorithms, because the scaling of the current equations does not change with the mobility values (see Table 4.1 on page 60). After careful consideration of those numerical difficulties, numerical parameters such as the correction step size, the convergence rate, the scaling values and the mesh size have been adapted. As a result, we have obtained the tweaked set of simulation parameters that is described hereafter and that we subsequently use as a reference case when further investigating other physical parameters in the later sections.

The design of the test device is inspired by early structures fabricated by Nakatsuka *et al.* [183]. This research group has indeed carried out investigations on the growth of GeSn layers from the beginning. The device consists in a 200 nm GeSn layer on top of a 500 µm Ge substrate, with Al electrodes and a NiGe(Sn) layer [184] between the top GeSn layer and the Aluminium contact (see Fig. 5.1). In order to account for the NiGe(Sn) - Aluminum contacts in the simulations, boundary conditions accounting for a Schottky barrier have been considered, whose value ϕ_b determines the (non-)ohmic character of the contact. A Schottky barrier height value of 0.2 eV has been

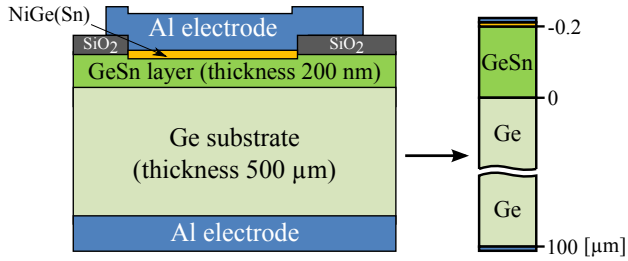


Figure 5.1: Unscaled schematic of the GeSn/Ge sample used in the reference simulations (right), based on devices fabricated by Nakatsuka et al.[183] (left).

used for the general case [185]. An arbitrary Shockley-Read-Hall trap energy level 100 meV above the valence band with a concentration of 10^{15} cm^{-3} is also included in the simulations, in order to assess the behaviour of the simulations with respect to such a trap state.

The thickness of the Ge substrate considered in the simulations has been limited to 100 µm in order to avoid unnecessary calculations and therefore improve the performance of the numerical simulation. The effect on the final solution is very limited, as most of the important microscopic variations occur within a few hundreds of nm from the GeSn/Ge interface. The only noteworthy impact is the proportional reduction of the series resistance of the substrate, roughly by the same factor of 5 as the size reduction. This will have to be taken into account when results involving the effect of series resistance are considered. A 0.6 eV bandgap energy for the GeSn layer has been used, obtained from interpolation of experimental and theoretical values found in the literature [64]. As GeSn is inherently p-type when undoped [183] and therefore more easily p-doped, be it with Boron implantation [20] or by in-situ Ga doping [186], p-type doping has been selected in the simulations for the GeSn layer, whereas the Ge substrate is n-type so as to obtain a pn junction. If not otherwise mentioned, the parameters used in the simulations are those listed in Table 5.1.

In the following simulations as well as in the electrical measurements of experimental devices, we used the convention that the contact connected to the Ge bottom substrate is considered as reference for the electric potential. A positive bias, $V > 0$, therefore means that the GeSn top layer is at a higher electric potential than the substrate.

Parameter	GeSn	Ge
Thickness	200 nm	100 µm
Sn concentration	5%	-
Bandgap	0.6 eV	0.7 eV
Typical carrier concentration	2×10^{18} cm^{-3} (p-type)	2×10^{17} cm^{-3} (n-type)
Trap concentration	10^{15} cm^{-3}	
Trap energy level	0.1 eV above the valence band	

Table 5.1: Physical parameters of the reference simulations.

Simulation of p-GeSn/n-Ge pn diodes

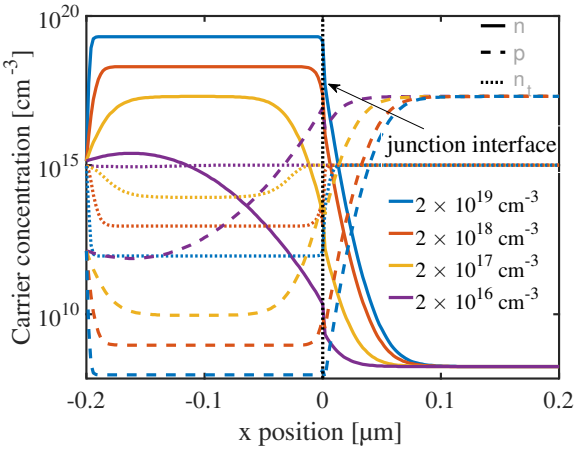


Figure 5.2: Static carrier concentration around the GeSn/Ge interface for several p-type dopant concentrations in the GeSn layer and 0 V bias.

The difference in doping type between the GeSn layer and the Ge substrate induces the formation of a depletion region, as depicted by the static carrier concentrations shown in Fig. 5.2. The drop of both electrons and holes concentrations in the vicinity of the heterojunction is clearly visible and the depletion region is seen to extend farther in the Ge substrate for higher p-

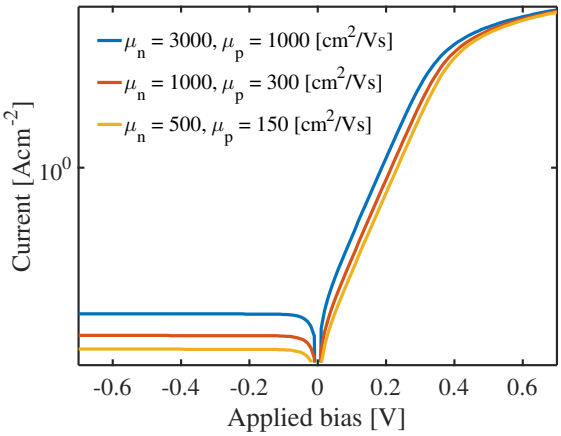


Figure 5.3: Current-voltage characteristics of GeSn/Ge diodes for different values of carriers mobilities.

type doping in the GeSn layer. This depletion region reveals itself as a major parameter controlling the current across the whole structure and it also allows the subsequent probing of its parameters by impedance spectroscopy.

Simulations with different values of carriers mobilities in the GeSn layer have subsequently been considered: high mobilities, $\mu_n = 3000$ cm^2/Vs and $\mu_p = 1000$ cm^2/Vs, which will be used in most of these simulations. These values are close to the bulk mobilities of Ge. Then we considered lower mobilities of $\mu_n = 1000$ cm^2/Vs and $\mu_p = 300$ cm^2/Vs, which are experimentally determined to correspond to the dopant concentration of 2×10^{18} cm^{-3} for the GeSn layer [20, 183]. And then half lower mobilities of $\mu_n = 500$ cm^2/Vs and $\mu_p = 150$ cm^2/Vs have been selected, so as to compare with a low mobility situation. There is therefore a ratio of approximately 6 between the low and high mobility cases. Figure 5.3 shows the I-V curve for the GeSn/Ge structure using these three different carrier mobilities in GeSn. The results indicate that the forward current increases with the mobilities, as expected from the direct dependence on the mobility in the theoretical current relation for a pn diode, Eq. (3.2) on page 23. The reverse current also increases with the mobilities, although it remains bias independent, thereby confirming that the mobilities only affect the reverse saturation current I_S.

The width of the depletion region at the heterojunction has an impact on the minimal thickness of the epitaxial GeSn layer required to perform sheet resistance measurements using a four-point probe [187], which can be

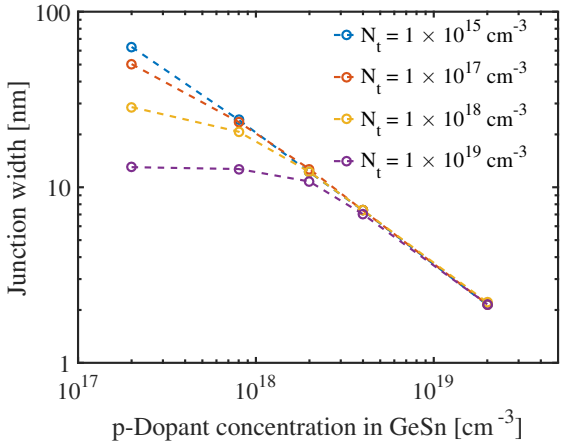


Figure 5.4: Depletion width on the GeSn side of a p-GeSn layer grown on a n-Ge substrate, as a function of p-type dopant concentration N_A in GeSn and for several trap concentrations N_t. Concentration dependent mobilities have been used.

useful for growth process tuning. To further exert these initial simulations, using calculations of the steady-state concentrations, we therefore estimated the minimum thickness as a function of p-type doping in the GeSn layer, as well as various trap concentrations N_t in the GeSn layer. Figure 5.4 shows these results, where doping concentration dependent mobilities in GeSn, extracted from experimental measurements, have been used. Mobilities of μ_n = 3000, 2000, 1000, 800 and 400 cm^2/Vs and μ_p = 600, 400, 300, 260 and 175 cm^2/Vs have been used for p-type doping concentrations of 2×10^{17}, 8×10^{17}, 2×10^{18}, 4×10^{18} and 2×10^{19} cm^{-3}, respectively [183, 20, 186, 188, 177]. This indicates that for thin GeSn layers, the depletion region might extend through the entire GeSn layer, especially for lower dopant concentrations in GeSn. The effect of the trap concentration in GeSn is similar to the increase of dopant concentration, reducing the width of the depletion region when its concentration increases. An apparent increase of the holes concentration indeed results from the trapping of electrons by the traps.

5.2 Samples

The GeSn layers used for the fabrication of the diodes were grown by CVD using digermane (Ge_2H_6) and tin-chloride ($SnCl_4$). A Boron-doped 200 nm

thick layer was grown at 320 °C on top of a 4", 450 µm thick Ge substrate using a 200 mm ASM-Epsilon™-like Reduced Pressure Chemical Vapor Deposition reactor [52, 20]. Blanket n-doped Ge(100) wafers with low ($\sim 10^{16}$ cm^{-3}) carrier concentration were used as substrates. The GeSn layer is *in situ* doped by adding B_2H_6 to the Ge_2H_6 and $SnCl_4$ precursors with a Boron target concentration of 3×10^{18} cm^{-3}. This target value is experimentally confirmed by secondary ion mass spectroscopy (SIMS) measurements and although B activation has not been measured on this specific sample, 100% B activation has been reported for similar GeSn layers [20].

According to (224) reciprocal space mappings (RSM) obtained from X-ray diffraction (XRD) measurements, the GeSn strain relaxation level is 43%. From the in-plane and out-of-plane lattice parameters measured by (224) RSM XRD, using a corrected Vegard's law, the substitutional Sn content in these layers is determined to be 5.8% [189]. This Sn content above 5% is located in the range of interest for strain engineering applications [177]. Al contacts with a thickness of 100 nm have subsequently been deposited by evaporation.

5.3 Electrical characterization

Electrical characterization of the diodes has been performed at room-temperature using an EPS150 probe station from Cascade Microtech. For temperature-dependent measurements, the diodes were glued with conductive epoxy to a sample holder with a Copper track for the backcontact. The top contacts were then wirebonded to custom printed circuit boards (PCBs) with coaxial plugs to allow for direct connection with coaxial cables.

5.3.1 Current-voltage characteristics

Room-temperature measurements

In order to assess the presence of traps in the electrical properties of the diodes, current–voltage (I–V) characteristics at room temperature have first been investigated. Figure 5.5 shows that the ratio between the current at +1 V and −1 V is 4 orders of magnitude. The forward current, in this vertically logarithmic plot, initially increases in a linear way, which indicates an exponential growth of the current with forward bias. This continues up to biases around +0.25 V, where the series resistance of the 450 µm Ge substrate starts to impact the I-V curve. The reverse current, on the other

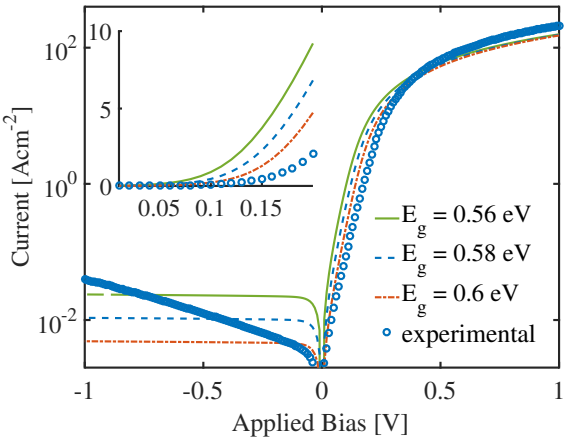


Figure 5.5: Room-temperature experimental and simulated I-V curves of the p-GeSn/n-Ge diodes. Three different GeSn bandgap energies are used for the simulations: 0.56 eV, 0.58 eV and 0.6 eV. Inset: enlarged view of the onset of the forward current.

hand, grows steadily with the applied bias, as opposed to the simple reverse saturation current of an ideal diode.

Simulations of structures similar to the experimental diodes have been run and are superimposed on the experimental data in Fig. 5.5, for three different bandgap energies of GeSn. These simulations show a total current matching for the forward bias. In reverse bias, though, the measured reverse current increases much faster than in the simulations. These simulated reverse currents are bias independent or at best linearly bias dependent, and therefore grow much more slowly than the measured reverse current, which shows more of an exponential behaviour. Their order of magnitude, however, fits the experimental data, using bandgap energies in the expected range for this GeSn layer [64]. In the simulations, the variation of the bandgap energy, which is related to the Sn concentration, shows that the reverse current increases when the bandgap energy decreases (*i.e.* the Sn concentration increases). This effect is related to the intrinsic carrier concentration n_i that increases exponentially when the bandgap energy decreases, and its direct impact on the reverse current saturation I_S. Even though the simulated reverse currents increase when the bandgap energy is lowered, the increase rate as a function of applied reverse bias remains much lower than the experimental one. Increasing the trap concentration of the GeSn layer on the simulations also gives rise to an increased reverse current, but not

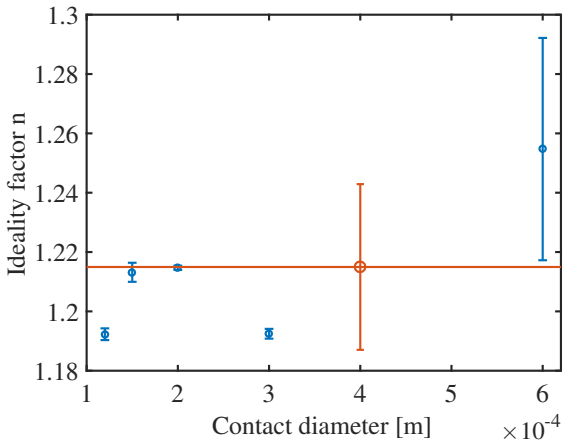


Figure 5.6: Ideality factor n of the p-GeSn/n-Ge diodes as a function of contact diameter, measured for several diodes of each diameter.

to the extent observed in the experimental data. The origin of this bias-dependent reverse current will be further discussed in a subsequent section of this chapter, using temperature-dependent measurements.

The ideality factor has been extracted from the forward I-V curves from diodes with different contact diameters. Biases restricted to a range between 0 V and +0.25 V have been used, in order to avoid the aforementioned effect of the series resistance of the Ge substrate. Values of n comprised between 1.2 and almost 1.3 are obtained, as seen in Fig. 5.6, depending on the contact diameter of the diode. The larger value is associated to the diodes with the larger contact diameter of 600 µm, whereas all other diameters between 120 µm and 300 µm result in a value of n between 1.2 and 1.22. The observed difference for the larger 600 µm diameter might originate from the higher total current flowing across the whole structure in this configuration. The current limitation due to the high resistivity of the thick, weakly doped, substrate, is therefore even more prominent. In order to overcome this issue, the bias range within which the ideality factor is extracted was further restricted so that the value of the coefficient of determination R^2 of the linear fit remains above 0.99. However, due to the earlier onset of current limitation for this larger contact diameter, a very slight difference in the slope of the linear fit can appear. Though not sufficient to degrade the R^2 value significantly, this could still lead to the observed difference of n values as compared to the other diameters.

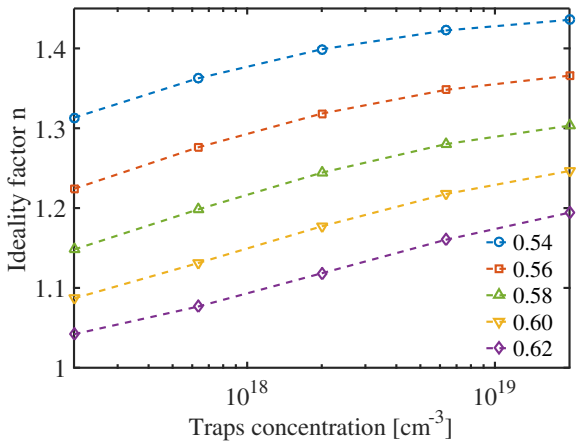


Figure 5.7: Impact of the trap concentration on the ideality factor n from simulations of GeSn bandgap energies between 0.54 eV and 0.62 eV and a Ge substrate dopant concentration of 1.5×10^{16} cm^{-3}. The energy unit has been omitted in the legend for the sake of figure clarity.

Overall, the mean value of 1.21 for the ideality factor is a clear indication of a close-to-ideal diode. Nevertheless, as an ideality factor n greater than unity is expected to point out the presence of recombination processes in the diodes, Shockley-Read-Hall (SRH) traps in the GeSn layer have been considered in the simulations used in view of a better understanding of the characteristics of these diodes. The included traps are expected to account for the presence of defects in the crystalline structure of the semiconducting materials under consideration. Bulk trap or interface traps can be investigated, depending on their spatial and energy position set in the simulations.

Figure 5.7 shows the impact of trap concentration on the ideality factor through simulations. Several values of the GeSn layer bandgap are also assessed. The ideality factor increases with the trap concentration, which is expected from their role as recombination centers in the depletion region. For a given trap concentration, the ideality factor also increases when the GeSn bandgap decreases. This behavior, likewise, is explained by the improved recombinations resulting from the smaller energy separation between the conduction and valence bands. As the bandgap energy of the GeSn epilayer is supposed to be around 0.58 eV for the Sn concentration of these diodes [55], the ideality factor close to 1.2 extracted from the experimental measurements would correspond to trap concentrations in the GeSn layer

comprised between 5×10^{17} cm^{-3} and 2×10^{18} cm^{-3}. This trap concentration, although relatively high, remains below the GeSn doping concentration and is therefore entirely conceivable.

Temperature-dependent measurements

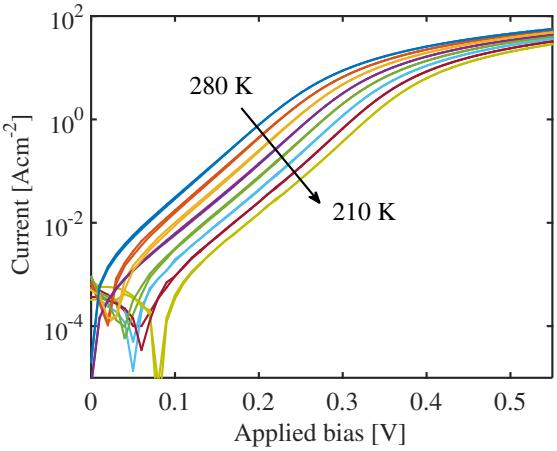


Figure 5.8: Experimental measurements of the forward bias I–V characteristics of the p-GeSn/n-Ge diodes for temperatures between 280 K and 210 K.

In order to further explore the mechanism at the origin of the observed reverse current, I-V characteristics as a function of diode temperature have been measured on a diode with a 300 µm diameter. I-V curves for temperatures ranging from 280 K to 210 K are shown in Fig. 5.8. The onset of forward-bias current is seen to shift towards higher positive values when the temperature decreases, as expected from the reduced thermal voltage $V_T = kT/q$. From these measurements, the ideality factor as a function of temperature has been calculated.

Figure 5.9 shows that the ideality factor goes from $n = 1.4$ at 280 K to $n = 2.8$ at 140 K, and is larger than $n = 2$ for temperatures lower than 180 K. This indicates that the current is not limited by drift and diffusion or by recombination in the depletion region anymore. Such processes, as band-to-band tunneling (BTBT) or trap-assisted tunneling (TAT), are not included in the numerical model used in the simulations, and this will be worth noting for the complete interpretation of the experimental results.

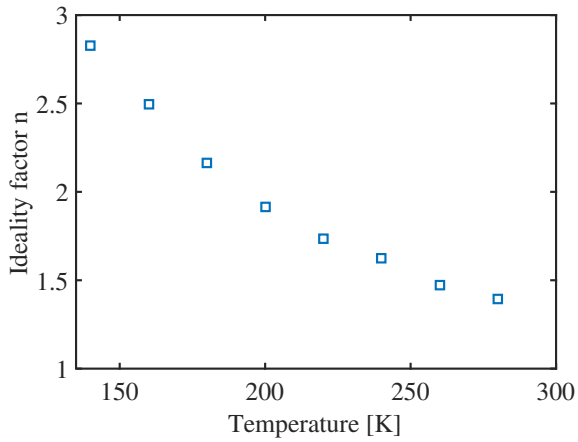


Figure 5.9: Ideality factor n of the p-GeSn/n-Ge diodes as a function of temperature for a contact diameter of 300 µm.

Reverse saturation current and interface states

From the I-V characteristics measured as a function of temperature, the activation energy E_a for the reverse saturation current I_S can be determined. Indeed, I_S can be expressed to be proportional to

$$I_S \propto e^{(-E_a/kT)}. \tag{5.1}$$

From the slope of an Arrhenius plot of $I_S(T)$ as a function of $1/kT$, the activation energy E_a can be extracted [190, 191, 192]. This activation energy is associated to the energy barrier that has to be overcome for the corresponding process to occur, namely the rise of the reverse saturation current. In the case of an ideal pn junction, this activation energy is linked to the intrinsic carrier concentration, which is itself dependent on the bandgap energy of the semiconductor.

From the first linear part at small forward bias of the I-V characteristics, the reverse saturation current I_S is extracted [111] as a function temperature, as was done for the ideality factor n in Fig. 5.9. The slope of the Arrhenius plot of these extracted I_S values as a function of $1/T$ yields an activation energy comprised between 0.28 eV and 0.30 eV, as shown in Fig. 5.10. The linearity of the Arrhenius plot is relatively good and the measurements are reproducible within the confidence interval given above. This activation energy lower than the bandgap of the materials in the pn junction indicates either a large band offset or the presence of traps at the interface [192]. A

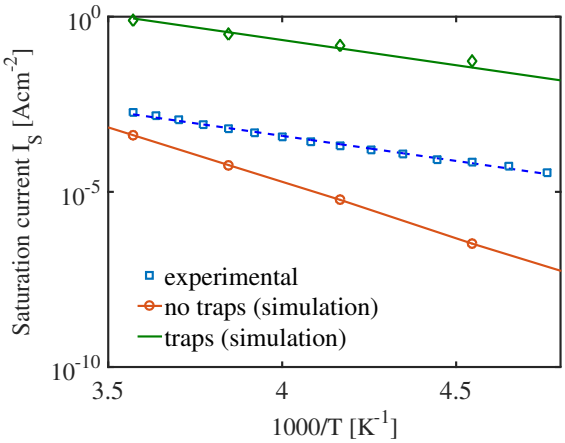


Figure 5.10: Extracted reverse saturation current as a function of the reciprocal temperature: experiment and simulations without defects and with defects extending 50 nm inside the Ge layer.

large band offset is quite unlikely in our case, as the GeSn and Ge bandgaps are not widely different.

To confirm these observations, a reference simulation of the diode structure, not including any traps, has been performed. From the complete I-V characteristics that are thus obtained, an Arrhenius plot has been constructed and yields an activation energy of 0.6 eV (see Fig. 5.10), close to the value of the bandgap energy used for the GeSn material. In addition, modifying the bandgap energy of the GeSn layer in the simulations induces a corresponding variation of the calculated activation energy. On the other hand, variation of the bandgap energy of the Ge layer does not induce any variation in the calculated activation energy. This result clearly indicates that the activation energy obtained in these simulations, in the absence of traps, is linked to the bandgap energy of GeSn.

Extraction of the activation energy from simulations including traps has subsequently been performed, in order to assess whether their presence can explain the experimental ~ 0.3 eV activation energy. We observed that the addition of traps in the GeSn layer did not lead to any difference in the obtained activation energy. When the traps are located in the Ge layer, though, the extracted activation energies change dramatically and can get closer to 0.3 eV. Traps extending over a few tens of nanometers from the GeSn/Ge interface and into the Ge substrate have therefore been further

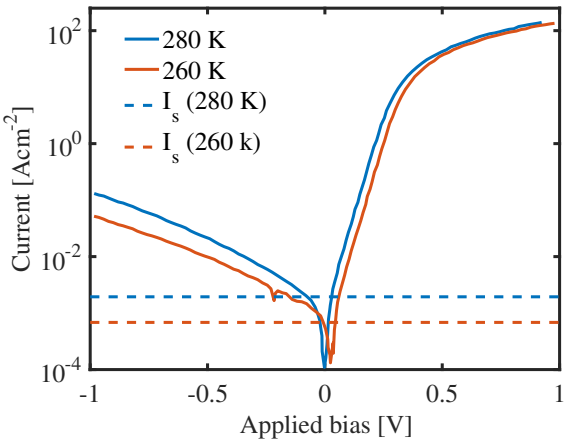


Figure 5.11: I-V curves of the p-GeSn/n-Ge diodes for temperatures of 280 K and 260 K and reverse saturation currents I_S extracted from the forward part of the I-V curve.

considered in order to get to an activation energy similar to the experimental one. Assessment of the effect of the various parameters of the traps lead us to determine that traps with a concentration of 2×10^{17} cm^{-3} and extending up to 50 nm inside the Ge layer are the best fit to the experimentally determined activation energy. As for their energy position, traps located between 200 meV and 250 meV above the valence band give activation energies closest to 0.3 eV (see the slopes in Fig. 5.10). Given the small extent of the traps and their concentration that is higher than the Ge substrate carrier concentration, these traps are therefore interpreted as interface states at the GeSn/Ge interface. Their presence could originate from the intermixing of GeSn and Ge, resulting in Sn-vacancy deep levels. Such a Sn-vacancy complex is expected to have an energy 190 meV above the valence band, as determined from combined DLTS measurements and ab-initio modeling of a Phosphorus and Tin doped Ge sample [193].

Regarding the general behaviour of the reverse current, the value of the reverse saturation current extracted from the linear part of the forward bias regime is located in the low range of the reverse currents that are experimentally observed, although an appropriate interpretation of the Arrhenius plot was unveiled by our analysis. From the I-V characteristics shown in Fig. 5.11, for instance, the extracted value of I_S at 280 K is 1.9×10^{-3} A cm^{-2}, while the experimental reverse current rises to 0.1 A cm^{-2} at -1 V. At 260 K,

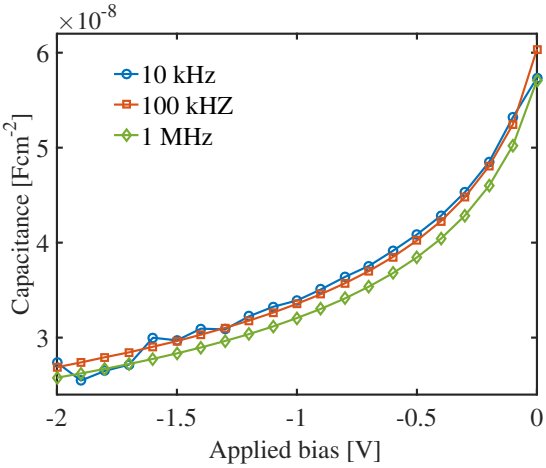


Figure 5.12: Frequency dispersion of the reverse C-V characteristics of the p-GeSn/n-Ge diodes with a 300 µm diameter.

the value of I_S is 6.8×10^{-4} A cm^{-2}, whereas the reverse current actually is 5×10^{-2} A cm^{-2} at -1 V. This suggests, in addition to the previously observed ideality factors n larger than 2 for lower temperatures, that the extracted activation energy of 0.3 eV and the associated traps at the GeSn/Ge interface do not account for the complete experimental behaviour of the devices. Because of the strong bias dependence of the total reverse current, additional effects such as trap-assisted tunneling or even band-to-band tunneling can be expected to play a role in the full behaviour of the devices [194]. From the previous observation of the higher than $n = 2$ ideality factor extracted from lower temperature measurements, trap-assisted tunneling is a highly plausible culprit, along with the possibility of field-enhanced recombinations through isolated point defects [195].

5.3.2 Capacitance-voltage characteristics

The impact of the previously identified traps on the capacitance-voltage (C-V) characteristics of those diodes has subsequently been assessed at various frequencies. Figure 5.12 shows the reverse-bias C-V characteristics measured at three different frequencies. A weak frequency dispersion is observed, indicating that the traps present at the GeSn/Ge interface do not have a strong influence on the frequency characteristics of the device. This is consistent with the fact that those traps are present in a narrow region near the GeSn/Ge interface, because the contribution of the traps to the

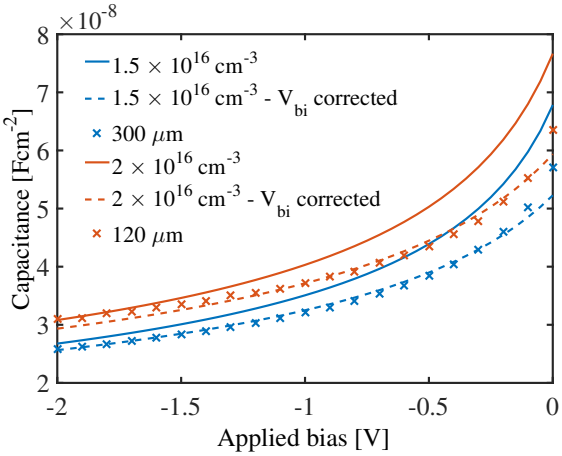


Figure 5.13: Capacitance as a function of applied reverse bias for two contact diameters of 120 µm and 300 µm. Both experimental and simulated curves are displayed, using carrier concentrations of 2×10^{16} cm^{-3} and 1.5×10^{16} cm^{-3} for the Ge substrate, respectively.

total capacitance is therefore very limited as compared to the depletion capacitance. As a consequence, the general behaviour of the capacitance as a function of applied bias is not significantly altered.

Experimental C-V characteristics have been measured for contact diameters ranging from 120 µm to 600 µm. Figure 5.13 shows both these experimental reverse-bias C-V characteristics and simulated ones for two contact diameters, 120 µm and 300 µm. A $1/C^2$ analysis has been performed and shows a very linear behaviour (Fig. 5.14), which is expected for a high-quality uniformly-doped material. Extraction of the active dopant concentration from the slopes of the $1/C^2$ plots yields values ranging from 1.4×10^{16} cm^{-3} to 2.4×10^{16} cm^{-3}, depending on the contact diameter and the measured diode. In the case of an asymmetric pn junction with one side that is much more heavily doped than the other, the extracted dopant concentration is that of the side with the lower concentration (see Eq. (3.13) on page 27). The value calculated in this analysis is therefore associated with the carrier concentration of the Ge substrate.

The general behaviour of simulated C-V characteristics is similar to the experiment, as shown in Fig. 5.13. The built-in potentials V_{bi} extracted from the simulations and the experimental curves are quite dissimilar, though, and

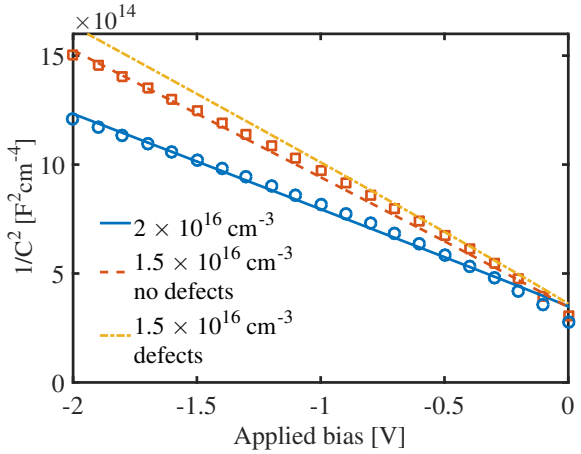


Figure 5.14: Comparison of the experimental $1/C^2$ for 120 µm (circles) and 300 µm (squares) diameters and V_{bi}-corrected simulated $1/C^2$ reverse-bias capacitance for two values of the carrier concentration in the Ge layer, with or without the presence of traps with a 2×10^{18} cm^{-3} concentration at the interface.

no parameter variation in the simulation could replicate the experimental built-in potential. Correcting the value of the simulated V_{bi}, *i.e.* shifting the simulation by a constant value, shows that the quadratic behaviour of both the measurements and simulations is identical, using fitting carrier concentrations in the simulations. It is also visible in the $1/C^2$ analysis of Fig. 5.14 that both the experiment and simulations demonstrate the same linear behaviour and slope. Only the x-intercept is different from the experimental one, but is corrected in the $1/C^2$ plot, too.

In these simulations, the addition of traps in the Ge layer close to the interface does not significantly modify the slope of $1/C^2$. Only when a concentration of traps as high as 2×10^{18} cm^{-3} is inserted does the slope begins to be altered, as shown in Fig. 5.14. This again tends to indicate that traps localized at the interface have a low effect on the C-V characteristics.

The local, microscopic, carrier concentration can also be observed in the simulations as a function of position. The depletion width can therefore be evaluated and is shown to be controlled by the applied bias. The depletion region also extends mostly in the Ge substrate, as expected from the much lower doping of the Ge substrate. When a larger reverse bias is applied, the depletion region widens and does so mostly on the Ge side of the GeSn/Ge

interface. The total value of the simulated capacitance is also directly linked to the width of the depletion region, thereby confirming the interpretation that the $1/C^2$ analysis gives access to the doping concentration of the Ge substrate.

Forward capacitance

Within the analysis of the simulated C-V characteristics, we also observed that, although the $1/C^2$ analysis only gives information on the doping concentration of the Ge substrate, the value of the maximum of the capacitance as a function of applied bias seemed to be related to the carrier concentration of the GeSn layer. This maximum capacitance occurs for small forward-bias values, as shown in Fig. 5.15. The maximum value of the capacitance in forward bias occurs at a different bias value, which depends on the GeSn layer carrier concentration. The value of that maximum capacitance also increases with the GeSn layer carrier concentration.

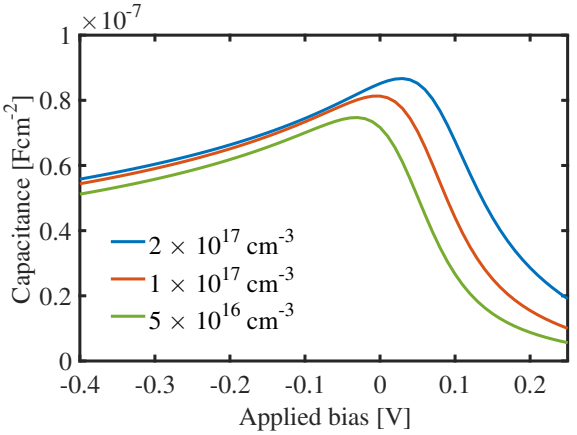


Figure 5.15: Diode capacitance at 1 MHz frequency as a function of the applied bias for carrier concentrations of 5×10^{16} cm^{-3} to 2×10^{17} cm^{-3} in the GeSn layer.

In order to assess the relationship between the value of the maximum capacitance in small forward regime and the carrier concentration in GeSn, we extracted the value of that maximum capacitance for several GeSn carrier concentration. The results, shown in Fig. 5.16, indicate that there is a direct linear relationship between the GeSn doping concentration and the maximum capacitance. This would theoretically allow to deduce the carrier

concentration of the more highly doped side of a pn junction. The linear relationship holds true for different measurement frequencies, although with another ratio. Increasing the frequency reduces the slope of the linear relationship. For lower concentrations, *i.e.* only one order of magnitude larger than the Ge carrier concentration, the relationship does not hold anymore, as shown in the inset of Fig. 5.16. Under these conditions, the maximum capacitance starts to be influenced by the carrier concentrations in both materials and the direct relationship with the GeSn carrier concentration is destroyed.

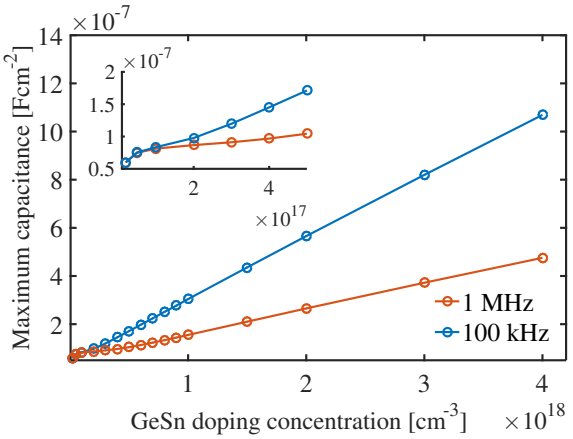


Figure 5.16: Maximum forward capacitance as a function of dopant concentration in the GeSn layer. Inset shows a magnification of the region of low concentration.

In order to ensure the relevance of those observations, the convergence conditions of those simulations have been checked and were of good quality. To further try to rule out a possible effect of numerical artefact, the tolerance on the convergence criteria was both relaxed or tightened, and the previous results could still be observed. The simulations give access to the amplitude of the local out-of-phase carrier concentration modulation, as shown in Fig. 5.17. We therefore probed whether the capacitance behaviour highlighted in this section could also be demonstrated from those microscopic quantities. Integrating the out-of-phase amplitudes over the entire semiconducting structure gives the total net charge modulation, which is directly linked to the small-signal capacitance $C = dQ/dV$. Our calculations to determine the maximum charge modulation (*i.e.* another way to calculate the

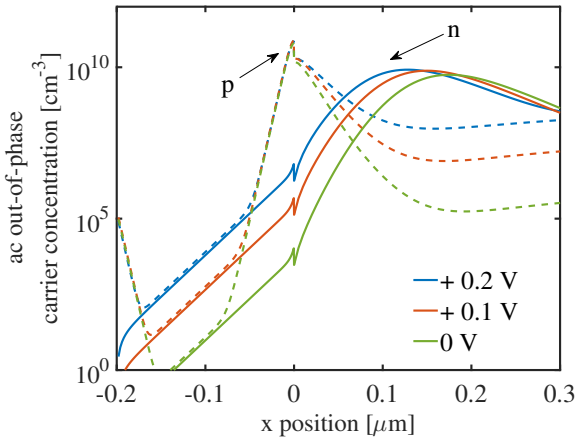


Figure 5.17: Microscopic out-of-phase ac variation of the carrier concentration of both holes and electrons as a function of position around the GeSn/Ge interface.

maximum capacitance) for various carrier concentrations in GeSn confirmed the link with the maximum capacitance.

Even though these were beyond the scope of this work, more investigations and comparisons with experimental results would be required to establish the potency of these observations. In particular, determination of the origin of the frequency dependence of the relationship would be required in order to unequivocally link a maximum capacitance value at a given frequency with a unique carrier concentration.

5.4 Effect of passivation on current transients in reverse-biased diodes

Proper passivation can have a dramatic impact on devices performance [70, 196]. Ge oxides suffer from water solubility and reduced thermal stability as compared to SiO_2, so that high quality passivation of these materials is a challenging process [197, 198, 199, 200]. Commonly used passivation techniques include [201, 202]:

- Growth of SiO_2 oxide on the sidewalls for a permanent and resistant passivation;
- HF or H_2O_2 exposure to obtain a temporary passivation;

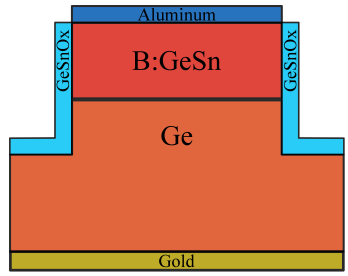


Figure 5.18: Schematic of the p-GeSn/n-Ge mesa diode in the absence of passivation.

- Performing the characterization of the device in a controlled atmosphere (e.g. Nitrogen) to avoid the contamination of the sidewalls and the growth of unwanted oxide.

In this section, we investigated mesa diodes structures, whose passivation is therefore a critical step in their process flow. We characterized the effect of a lack of passivation on GeSn/Ge mesa diodes to assess the impact on the electrical characteristics due to the growth of a few nm of $GeSnO_x$ native oxide. We specifically examined whether we could have access to electrical characteristics close to those of the passivated diodes.

Mesa diodes preparation

p-GeSn/n-Ge mesa diodes, as schematically depicted in Fig. 5.18, have consequently been fabricated, based on the same substrates and GeSn layers as in the previous section [20]. The preparation of the mesa diodes included the following steps:

- 2% HF dip for 20 seconds to remove the native oxide;
- Thermal evaporation of 100 nm Al using hard mask;
- Backside metal deposition of 100 nm Au by thermal evaporation;
- Dry Reactive-Ion Etching (RIE) using SF_6 + O_2 to etch the GeSn layer, using the Al contact as etch mask.

Following these steps, the sidewalls of the diodes were left unpassivated. The growth of a few nm of (possibly non-stoichiometric) $GeSnO_x$ is therefore expected to occur.

Consequences of a lack of passivation

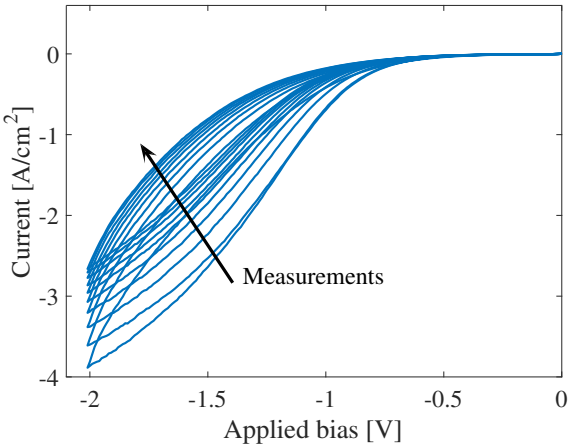


Figure 5.19: Repeated I-V measurement of unpassivated p-GeSn/n-Ge diodes between −2 V and 0 V.

Figure 5.19 shows repeated I-V measurements between −2 V and 0 V, performed on such an unpassivated diode. The amplitude of the hysteresis is particularly large between around −1 V and −2 V, with over 50% more current going from 0 V to −2 V than back from −2 V. The maximum (in amplitude) reverse current that is reached at −2 V is also decreasing after each repeated measurement. Although the reduction in current at −2 V after each measurement decreases for each new measurement, a stable value is not reached even after many measurements. In the forward bias regime, the measured current is obviously much larger, but no significant hysteresis is observed.

Time measurements have also been performed, recording the current at a fixed reverse bias of −2 V for as long as one hour. In Fig. 5.20, the current first increases (in amplitude) quite fast for a few tens of seconds and then starts to decrease, on a much slower time scale. A few seconds after the start of the first measurement, the current is as high as −1.63 A/cm^2, while after 60 minutes, it has become up to 50% lower, at almost −0.8 A/cm^2. Repeating the same 1-hour measurement cycle after the first one shows the same behaviour, with a fast initial increase of the reverse current followed by a much slower decrease of the measured current. Some memory effect also affects the characteristic, as indicated by the reduced overall measured current in the second measurement. As will be further discussed below, this

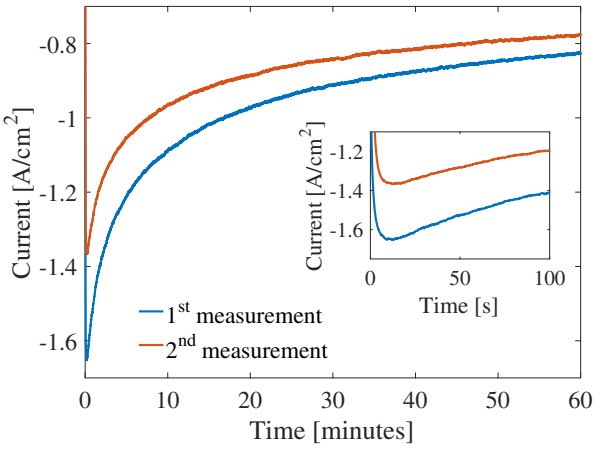


Figure 5.20: Successive time measurements of the current measured at -2 V bias on unpassivated p-GeSn/n-Ge diodes. Inset: zoom on the first 100 s of the transients.

memory effect can remain present for a very long time after any electrical measurement is applied to the diodes.

Temporary passivation

As previously indicated, we attribute these effects to the charging/discharging of traps in the oxide of the sidewalls. To confirm that hypothesis, we tried to temporarily remove the native oxide from the sidewalls. We dipped the diodes in dilute hydrogen peroxide (H_2O_2) for 30 seconds and immediately performed the electrical measurements again.

The results are shown in Fig. 5.21: the large transient has completely disappeared as compared to the measurement before the H_2O_2 dip. We expect that the removal of the native oxide has eliminated the conduction through the sidewalls. In the absence of this alternate conduction pathway, the stable current measured is four times lower than the maximum current measured in the previous transients. This comes as a confirmation that those transients are linked to conduction through the sidewalls.

The I-V characteristics of the H_2O_2 passivated diode is displayed in Fig. 5.22. From the forward-bias part of the curve, the ideality factor and reverse saturation current I_S have been extracted. The series resistance R_S has been accounted for by using the following relationship:

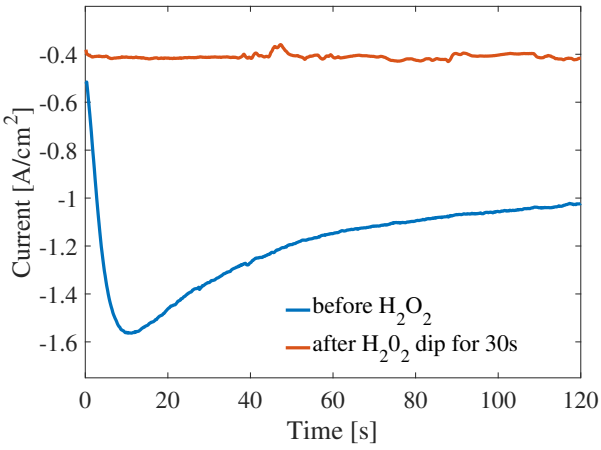


Figure 5.21: Time measurements of the current measured at -2 V bias, performed on the diode before and after the H_2O_2 temporary passivation.

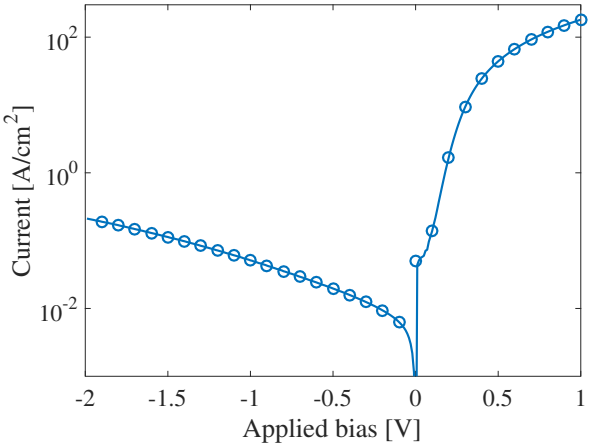


Figure 5.22: I-V characteristics of the H_2O_2 passivated p-GeSn/n-Ge mesa diode.

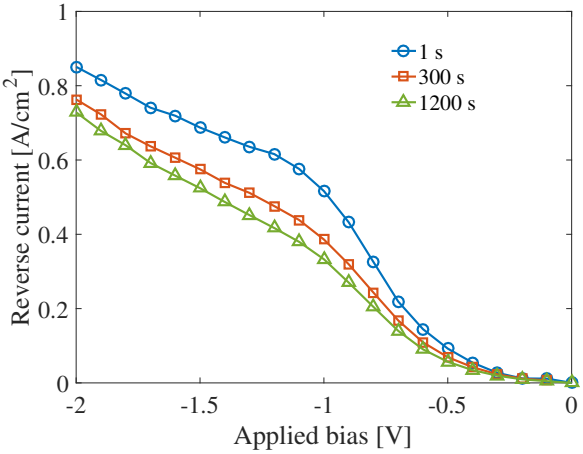


Figure 5.23: Reconstructed I-V characteristics of the unpassivated diode by using the current obtained after 120 seconds at each bias, for several diode temperatures.

$$I = I_S \exp\left(\frac{V - IR_S}{V_{th} n}\right). \tag{5.2}$$

Values of $n = 1.8$ and a reverse saturation current $I_s = 1.91 \times 10^{-2}$ A/cm^2 are extracted. This indicates that, although the H_2O_2 passivation dramatically reduced the time transient in reverse-bias regime, the effects of recombination are still prominent in these mesa diodes. This observation is in line with the results from the characterization of the diodes in the first sections, which are based on the same GeSn/Ge layers.

Large current transients in unpassivated diodes

The large transients observed in reverse bias in the absence of passivation are several times larger than the values measured on diodes passivated by an H_2O_2 dip. After an initial fast growth of the measured current, follows a much slower reduction of the measured current (see Fig. 5.20). We therefore performed measurements at a fixed bias of -2 V for increasingly long times in order to try and reach a steady value for the current. No stable value could be reached, though, even after applying the -2 V bias for as long as 12 hours.

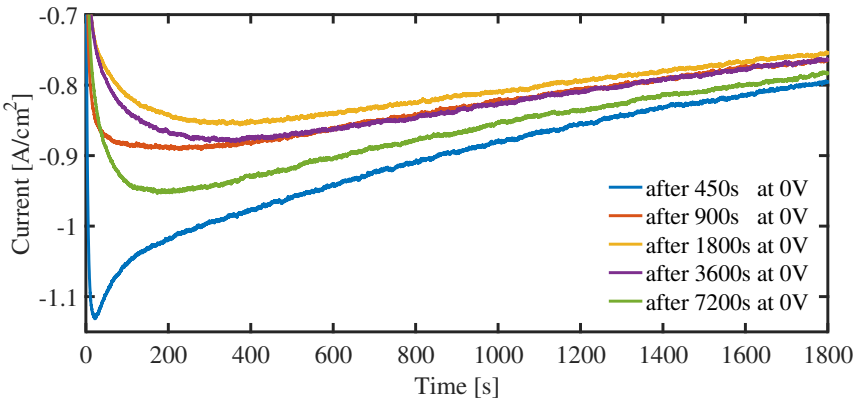
We subsequently attempted to reconstruct I-V characteristics for the diodes from the current obtained after leaving the diode biased for preset time

durations. Figure 5.23 shows these reconstructed I-V characteristics, with three different waiting times before recording the current value: 1 second, 5 minutes and 20 minutes. The results show that, especially for reverse biases beyond −1 V, there is a large variation in the shape and values of the curve depending on the length of time elapsed before the measurement. The values get more similar between each other as the waiting time increases, as already observed in the transients for one fixed bias, but repeatable curves cannot be obtained by waiting even for very long times.

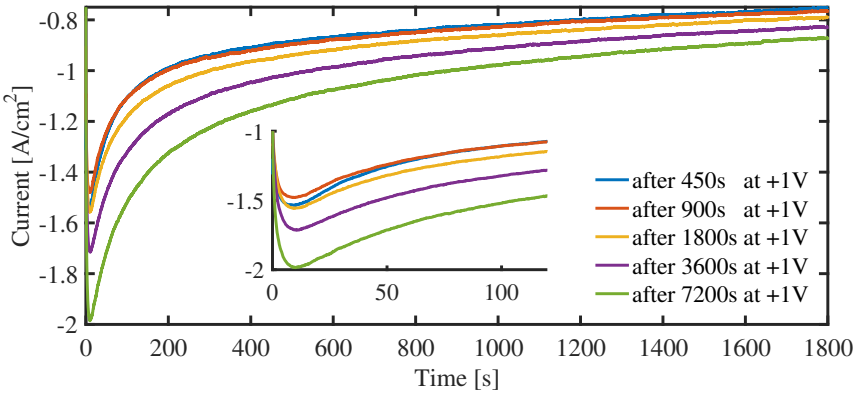
As each measurement also seems to impact the subsequent measurements, we investigated the effects of several repeated transient measurements. The general effect of one measurement on the next is to decrease the amplitude of the subsequent transient, so we explored the consequences of changing the conditions applied to the diode in-between the successive measurements. The procedure is as follows: the diode is biased at −2 V for 30 minutes (1800 seconds) and then shorted (0 V applied between the contacts) for a given time t_{short} before repeating the measurement at −2 V for 30 more minutes, and so on. The time t_{short} that the diode is left in short circuit is increased after each measurement and takes successive values of 7.5 minutes (450 seconds), 15 minutes (900 seconds), 30 minutes (1800 seconds), 60 minutes (3600 seconds) and 120 minutes (7200 seconds). Fig. 5.24 (a) shows those successive transients, where it can be observed that for the first three measurements (up to 30 minutes at 0 V between measurements), the amplitude of the transient decreases after each new measurement. Starting from resting-times at 0 V of 60 minutes and beyond, the transients become larger again.

The same experiment has been performed, using resting-conditions that now consist in biasing the diodes in forward, at +1 V, instead of leaving them in short-circuit at 0 V. Fig. 5.24 (b) shows this experiment and in this case, the transients do not decrease in amplitude even for the shortest times spent at +1 V. They also start to get larger for +1 V biasing times as short as 30 minutes, half the time required when leaving the diode at 0 V to obtain the same result.

Biasing of the diode in forward at +1 V obviously enables the recovery of a transient whose amplitude is similar to or even larger than the initial one. We therefore measured the current reached after biasing the diodes at −2 V for 15 minutes, which is done after the biasing of the diode for an increasingly long time at +1 V. Figure 5.25 shows the results, indicating that a stable final current cannot be reached, even though the diode has been polarized at +1 V for up to 2 hours. Successive measurements at −2 V shift the current



(a)



(b)

Figure 5.24: Time measurements at -2 V for 30 minutes, (a) with increasingly long time spent at 0 V between successive measurements and (b) with increasingly long time spent at $+1$ V between successive measurements. Inset: zoom on the first 120 s of the transients.

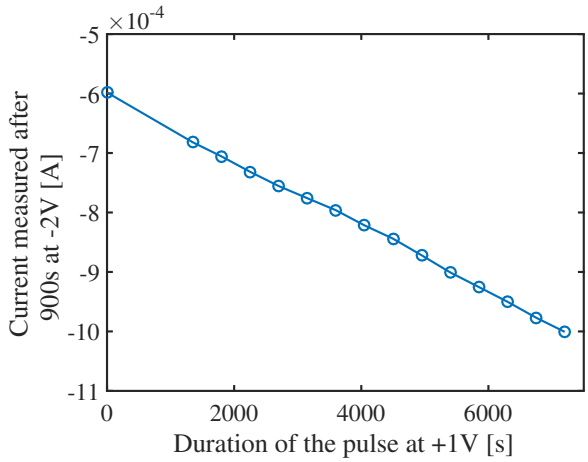


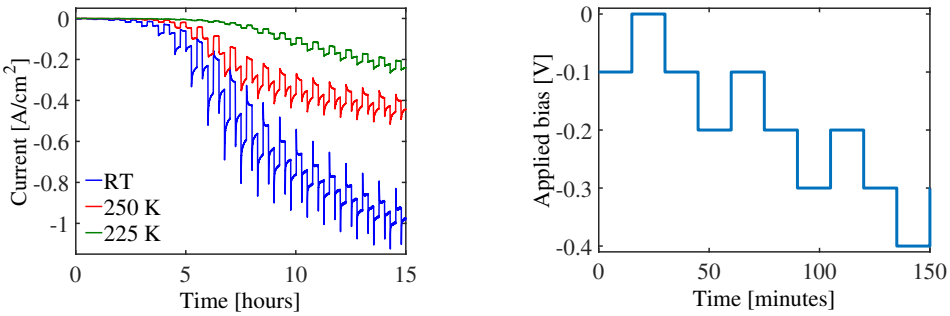
Figure 5.25: Evolution of the current reached after 15 minutes at -2 V as a function of the time that the diodes has been biased at $+1$ V before the measurement.

to lower absolute values, whereas biasing the diode at $+1$ V increases the current subsequently measured at -2 V in absolute value, but it does so in a way that can go beyond the initially measured current. Returning the diode to an "initial" state, free of the influence of the previous measurements, therefore does not seem possible. This behaviour is, however, another clear indication of a mechanism of charging and discharging of traps, located in the native oxide on the sidewalls. Although only qualitative results are obtained from these measurements, the large transients imply a high trap concentration and given their very long memory effect, the time constants of those traps are also expected to be very large.

Effect of temperature and applied bias

In order to further evaluate the properties of those traps and the behaviour of their related transients, we extended the range of measurement conditions to include the variation of temperature as well as the dependence on the reverse-bias applied to the diodes.

A new time measurement protocol has been devised, where the bias applied to the diode is swept from 0 V to -2 V by steps of 0.1 V. In addition, after a first measurement at step i, and before going to the next bias step $i+1$, the bias is set back to the previous step value $i-1$, followed by a second time at the current step i and finally to step $i+1$. All steps are measured



(a) (b)

Figure 5.26: (a) Time evolution of the current measurement for biases switching back and forth by 0.1 V steps up to −2 V, at room temperature, 250 K and 225 K. (b) Time evolution of the bias applied to the diode in the experiment depicted in (a).

for 15 minutes and the total measurement takes more than 15 hours. To better explain the values of the successive bias steps, Fig. 5.26 shows the time dependence of the applied bias: starting from a time measurement at −0.1 V, the bias goes back to 0 V, then back again to −0.1 V and on to the next step at −0.2 V. This procedure allows to characterize the transients associated with a step bias change of 0.1 V, both from over and below, for each applied bias between 0 V and −2 V. This measurement procedure, which lasts up to 15 hours, has been performed at various temperatures. Figure 5.26 shows the results for three different temperatures of the diode: room-temperature, 250 K and 225 K.

The transients are relatively small in amplitude at the beginning of each measurement, which corresponds to low reverse biases. They subsequently grow in amplitude, especially for the room-temperature measurement. To better visualize this evolution, we define the amplitude of the transient as

$$\text{transient amplitude} = \frac{\text{peak value - final value}}{\text{final value}} \tag{5.3}$$

and report it in Fig. 5.27, where "peak value" is the maximum current (in absolute value) measured during that transient and "final value" is the current measured at the end of the 15 minutes transient. Figure 5.27 clearly shows that the amplitude of the transients increases with the applied reverse bias for all temperatures, although the overall amplitude decreases with the diode temperature. Large transients are observed at room-temperature starting

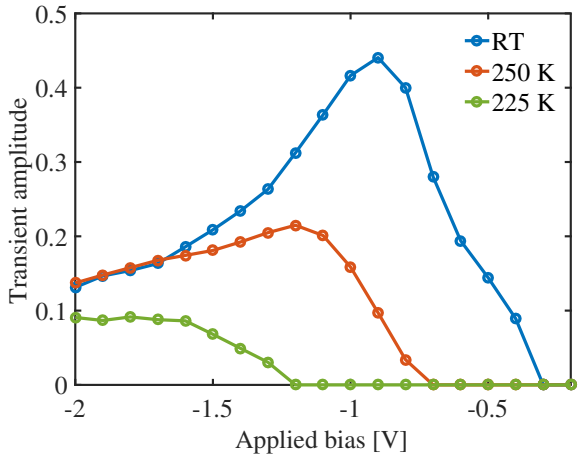


Figure 5.27: Amplitude of the transient associated to a 0.1 V bias change as a function applied bias, for three diode temperatures: room-temperature, 250 K and 225 K.

from −0.8 V, whereas more and more negative biases are necessary to obtain large transients at 250 K and 225 K. It is also to be noted that, because of the chosen definition for the transients amplitude, the calculated value can be zero even though there *is* a transient, as is the case for transients at biases above −0.7 V and −1.2 V for 250 K and 225 K, respectively. The zero amplitude value indeed only indicates that the final current value *is* the peak value reached during the transient. In order words, a zero amplitude points out a monotonously decreasing transient, as opposed to the other, two steps, transients.

The transients also reach a maximum amplitude for some bias, and this value shifts to more negative biases for lower temperatures. An unsubstantiated explanation for this behaviour could reside in the competition between the current actually flowing through the diode and the current flowing through the native oxide on the sidewalls. At first and for low reverse biases, the current that can flow through the actual diode is small, so that a large current can flow through the native oxide and charge traps located inside it. The reverse current flowing through the actual diode increases steadily with the applied bias, though, even on the temporarily passivated diode (Fig. 5.22). Starting from the bias where the transient amplitude is maximum, the current in the actual diode might therefore reach a value such that the electric field applied to the traps in the oxide is actually reduced, and less of those traps get consequently charged, reducing the transient

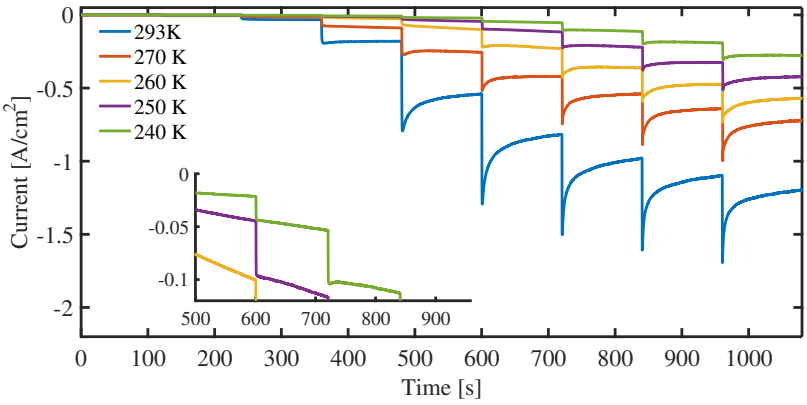


Figure 5.28: Successive 120 seconds long transients between 0 V and −2 V by 0.25 V steps, for temperatures between 293 K and 240 K.

amplitude. Another possibility could result from the experimental procedure, that only brings the potential one 0.1 V step back before going on to measure the next transient. Starting from biases of, e.g. −1 V at RT, most of the traps could have already been charged, or insufficiently discharged by the 0.1 V step back, to allow the observation of the transient with its complete amplitude.

An ultimate experiment, consisting in time measurements with monotonously decreasing biases from 0 V to −2 V, with a bias step of 0.25 V and a duration of 120 s, is shown in Fig. 5.28. The time measurements are repeated for temperatures from 293 K to 240 K and show, as before, that the transients amplitude is strongly temperature-dependent. The transients are very large at room-temperature and their amplitude is considerably reduced for temperatures as low as 240 K. This measurement allows to calculate an activation energy for the final current obtained after 120 s at each bias step, which is displayed in Fig. 5.29.

This activation energy shows a maximum value for biases around −1 V and decreases for biases beyond that value, in the same way as the transient amplitude in Fig. 5.27. This activation energy is related to the barrier that has to be overcome in order to reach the current measured after 120 s. It therefore makes sense that the maximum activation energy is required for biases around −1 V, where the transients amplitude are also at their maximum.

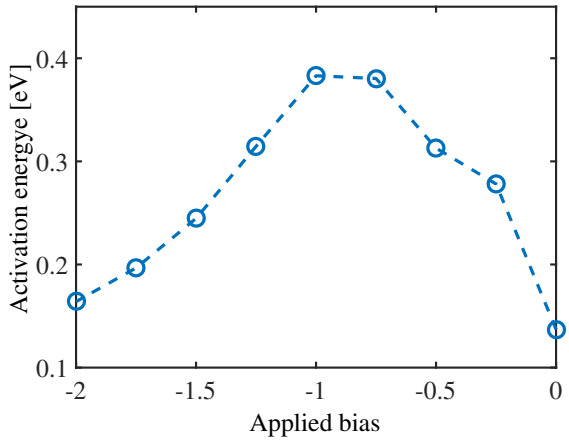


Figure 5.29: Activation energy of the transients as a function of applied reverse bias, for temperatures between 293 K and 240 K.

Modelling of the sidewall conduction

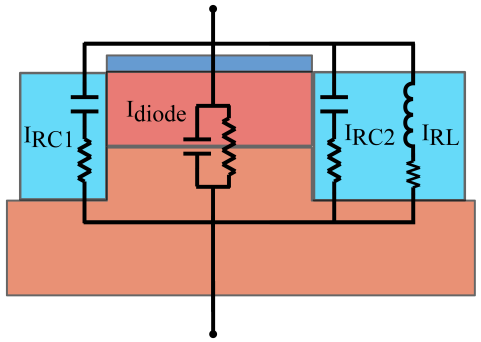


Figure 5.30: Schematic of the electrical RC model of the conduction through the p-GeSn/n-Ge mesa diode as well as the native oxide on the sidewalls.

Following these experiments and observations, we modeled the assumptive sidewall conduction mechanism through the oxide by capacitors and resistors in series, as is shown in Fig. 5.30. The addition to the model of a given RC branch leads to a decaying exponential resulting current I_{RC}, along with a corresponding time constant τ_{RC} of the form: $I_{RC} \propto -\exp(-t/RC) = -\exp(-t/\tau)$. To model the presence of a distribution of time constants, the

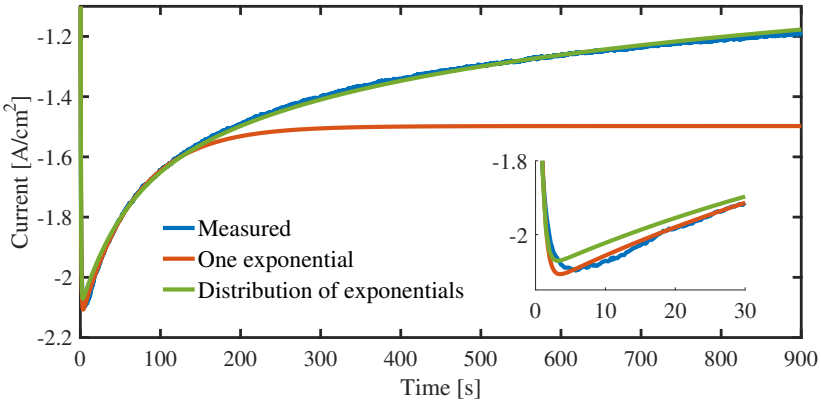


Figure 5.31: Modelling of the sidewall conduction through the native oxide of the mesa diode for a single time constant and a distribution of exponentials. Inset: zoom on the first 30 s of the transients.

total current is therefore modeled by a sum of exponentials. The initial fast transient, on the opposite, is modeled by an inductive component with time constant τ_{RL}, inducing an exponentially increasing current component I_{RL} (see Fig. 5.30). The physical interpretation of this inductive component is linked to a long transit time of charges across the oxide. The total dependence as a function of time for the current across the mesa diode and native oxide on the sidewall is therefore expressed as

$$I_{\text{total}}(t) = I_{\text{diode}} + I_{RL} + \sum_n I_{RCn} \tag{5.4}$$

$$= I_{\text{diode}} + \exp\left(\frac{-t}{\tau_{RL}}\right) + \sum_\tau - \exp\left(\frac{-t}{\tau}\right) \tag{5.5}$$

where I_{diode} is the current actually flowing through the diode itself and not through the sidewalls.

Modeling with a single RC time constant, as shown in Fig. 5.31, allows to fit the early part of the experimental transient at -2 V, but the current becomes constant much earlier than in the experiment. The best fit for a single time constant is obtained with a value of $\tau \sim 150$ seconds. Using a distribution of time constants ranging from 10 seconds to 10^6 seconds ($\sim$ 10 days) allows to fit the data much better, as shown in Fig. 5.31. Regarding the initial inductive part of the current, I_{RL}, time constants of the order of

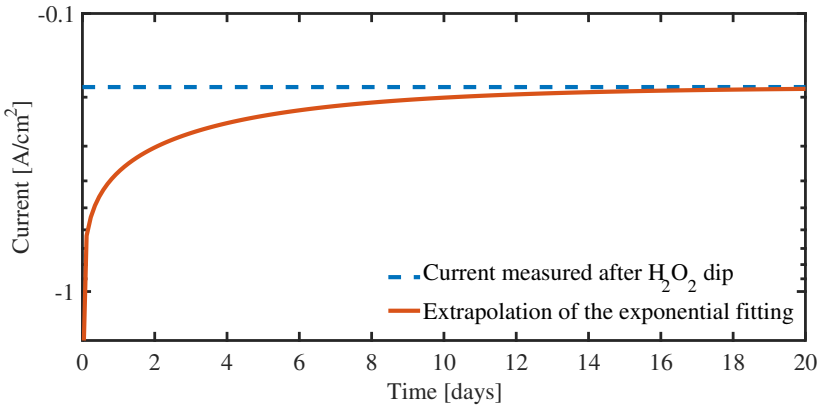


Figure 5.32: Extrapolation of the exponential fitting of the transient with a distribution of time constants for 20 days, compared to the steady current measured at -2 V after passivation with H_2O_2.

10^{-3} s are repeatedly obtained. This order of magnitude equates to an average speed of 0.2 cm/s. It is consistent with values reported for the transit time of charges through an oxide [203], although those values can easily differ over of a few orders of magnitude, depending on the parameters of the oxide.

The steady state current obtained after charging all the capacitors in the model can also be estimated from the fit. Values several times smaller than the initial transient current are obtained. Using the distribution of time constants, an additional constraint can be set on the final current so that it is equal to the current measured with the diode after passivation. The model can subsequently be extrapolated over a very long time (days) to estimate the time necessary to charge all the traps in the sidewalls. A time period longer than 2 weeks is obtained (see Fig. 5.32), after which one could hope to be able to measure a current similar to the passivated reverse current at -2 V.

5.5 Conclusions

In this Chapter, simulations of GeSn semiconducting materials are introduced along with the parameters used in the later calculations. Boron doped p-GeSn/n-Ge diodes grown by CVD with 5.8% Sn concentration have subsequently been investigated. The measured electrical characteristics reveal

good-quality diodes, with little effect of the presence of traps in the structure. An ideality factor at room temperature of 1.2 indicates the occurrence of limited recombinations. Through temperature measurements and simulations, an activation energy of approximately 0.3 eV is determined for the reverse saturation current I_S, as a result of the presence of recombination centers in the space charge region.

Simulations indicate that the associated traps are likely to have an energy level situated around $200 - 250$ meV above the valence band, similar to the expected energy of Sn-vacancy deep levels. Strong bias-dependence of the reverse current is also noted, denoting that an additional, field-enhanced mechanism such as trap-assisted tunneling (TAT) or even band-to-band tunneling (BTBT) is also present. The carrier concentration in the Ge layer is determined by C-V measurements and little frequency dispersion is observed, in spite of the traps assumed to be present at the GeSn/Ge interface. A link between the maximum of the capacitance at small forward bias and the dopant concentration in the GeSn layer is also highlighted by the simulations of the C-V characteristics.

In a second part, the electrical response of unpassivated mesa diodes is studied. A strong hysteretic behaviour is observed in reverse bias, as well as large transients when measuring the current flowing through the diodes over time at a fixed reverse bias. Dipping the diodes in H_2O_2, which effectively passivates the diodes by removing the native oxide on the sidewalls, results in the complete disappearance of the hysteretic behaviour and the transients.

On the unpassivated diodes, several different conditions have been tested between successive measurements in order to try to obtain repeatable measurements. Shifting of the transients both to larger or smaller currents depending on the applied conditions makes it impossible to obtain a steady, repeatable response of the unpassivated diodes with usual measurement techniques. The effect of temperature, which is shown to play a role in the activation of the amplitude of the transient response, is also noted. The transients are larger for reverse biases beyond -1 V and up to -2 V. A maximum activation energy is noted for a reverse bias of -1 V, which suggests a competition mechanism between charging of the traps in the native oxide on the sidewalls and the current flowing through the actual diode.

Finally, modelling of the transient responses with an equivalent electrical circuit containing a series of RC elements is investigated. A distribution with continuously spaced time constants is found to be necessary to reproduce the shape of the transients. Extrapolation of those results along with the

current value observed on the H_2O_2 passivated diodes indicates that the transient response might take over 2 weeks before all traps in the native oxide on the sidewalls are completely charged and a steady current can be measured.

Chapter 6

GeSn based MOS structures

Parts of this chapter have been published in the following articles :

- **Baert, B.**, Schmeits, M., & Nguyen, N. D. (2014). Study of the energy distribution of the interface trap density in a GeSn MOS structure by numerical simulation of the electrical characteristics. *Applied Surface Science*, **291**, 25-30. http://hdl.handle.net/2268/156365
- Wirths, S., Stange, D., Pampillon, M.-A., Tiedemann, A., Mussler, G., Fox, A., Breuer, U., **Baert, B.**, San Andres, E., Nguyen, N. D., Hartmann, J.-M., Ikonic, Z., Mantl, S., & Buca, D. (2015). High-k Gate Stacks on Low Bandgap Tensile Strained Ge and GeSn Alloys for Field-Effect Transistors. *ACS Applied Materials and Interfaces*, **7**, 62-67. http://hdl.handle.net/2268/196534

Accurate characterization of defects states at the interface between oxides and semiconductors is of tremendous importance for the development of GeSn-based MOSFETs. Techniques such as the conductance method or the systematic identification of typical features in C-V curves have been routinely used with success for the characterization of silicon devices. They cannot be directly applied to structures made out of new materials such as GeSn, though, without paying careful attention to the possible difficulties that arise from their specific material properties.

It has already been shown that in low bandgap materials such as Ge, the interface trap density can be easily under- or overestimated [141, 137]. The weak inversion and depletion responses can be easily confused. Moreover, there are technical constraints linked to the interface trap constants, the extraction of the energy-voltage relationship can be difficult and sensitivity to high interface trap densities can be lowered. Some of these issues are directly related to the lower bandgap of the investigated Ge materials. In the conductance method, for instance, the response due to weak inversion is enhanced by the stronger interaction of the traps with both minority and majority carriers. The ability to probe a wider range of energies within the bandgap for interface trap densities, however, is improved for lower bandgap materials, because the Fermi level can be proportionally moved further within the bandgap.

The bandgap of GeSn materials is even smaller than that of Ge. It is therefore expected that those issues will also be present, possibly with an even larger impact, when applying common characterization techniques on GeSn MOS structures. Using the numerical simulation tool presented in Chapter 4, we investigated the key elements in the theoretical electrical signatures of interface traps in such structures made of small-bandgap materials under ac regime. The aim is to clarify in a comprehensive way the role of interface traps in electrical characteristics such as C-V and impedance spectroscopy, which are dominantly used by all device makers.

After the presentation and discussion of the specific issues related to the numerical simulations of these structures, the C-V characteristics of MOS structures in presence of interface traps are investigated in Section 6.2. Then, in Section 6.3, the conductance method is discussed in the presence of discrete and extended energy traps. The interface traps time constant is also examined. The impact of the bandgap energy and other parameters on the onset of the inversion response is analyzed in Section 6.4. Finally, two experimental MOS samples are presented and briefly discussed in Section 6.5. A link between the features observed in the impedance data and the traps

characteristics is established. More details on these samples are given in Appendix D.

6.1 Simulation of interface traps in MOS structures

The simulations performed in the following sections are based on the numerical tool detailed in Chapter 4. A few additional remarks pertaining to the specific modeling of MOS structures are discussed here. First, the oxide is represented as a very large bandgap material with no doping. This makes it essentially isolating, while still following the general formalism and behavior of the numerical simulation of semiconducting materials. The bandgap difference with the semiconducting material (*i.e.* GeSn in this case) is assumed to be evenly distributed between the valence and conduction bands offsets. This arbitrary choice is allowed by the large bandgap difference between the oxide and the semiconductor.

Modeling of the traps at the interface between the oxide and the semiconductor is performed by the inclusion of a bulk trap state with a given energy in the semiconductor bandgap. To make it an *interface* trap, its spatial extension is limited to within 3 nm from the interface, on the semiconductor side. The input density is therefore a volumic concentration, which is integrated over 3 nm to obtain the corresponding surface density of the traps at the interface.

GeSn materials are known to be inherently p-type materials when they are undoped, or unintentionally doped. The semiconductor side of the MOS structure has therefore been assigned a p-type carrier concentration of 10^{17} cm^{-3}, similar to values measured on other undoped GeSn layers [204]. The bandgap of the GeSn layer is taken as 0.6 eV, corresponding to an approximate Sn concentration of 5% [64], which is the content expected to be required to obtain competitive high mobility GeSn materials [177].

The other physical parameters used in the simulations, if not otherwise mentioned, are listed in Table 6.1.

Numerical convergence of the simulations is sometimes very challenging, especially for high biases in the presence of high densities of defects at the interface. This troublesome convergence is directly related to the high variations of carrier concentrations at the interface, from the accumulation of charges at the traps to the almost-zero carrier concentration in the oxide. Low temperatures also make the convergence harder, by further altering the

Parameter	Symbol	GeSn value	Al_2O_3 value
Temperature	T	300 K	
Thickness	t	100 nm	14 or 9 nm
Doping concentration	N_A	10^{17} cm^{-3}	-
Bandgap	E_g	0.6 eV	6.5 eV
Sn content	x	5%	-
Dielectric constant	ϵ_r	16.3	9.3
Electron mobility	μ_e	3000 cm^2/Vs	-
Hole mobility	μ_p	1000 cm^2/Vs	-
Traps:			
Electron capture cross section	σ_s^p	10^{-16} cm^2	
Hole capture cross section	σ_s^p	2×10^{-16} cm^2	

Table 6.1: Microscopic parameters used for the simulations of MOS capacitor structures.

equilibrium between the Fermi potentials and k_BT/q in the exponentials expressing the carrier concentrations. The simulated curves presented below are therefore sometimes not entirely complete towards large positive biases, for some combinations of microscopic parameters.

6.2 Capacitance-Voltage characteristics

C-V characteristics of GeSn materials have been numerically simulated in the presence of traps, at first arbitrarily located 250 meV above the valence band, in view of assessing their effect on these C-V characteristics.

Figure 6.1 shows these C-V characteristics for frequencies from 1 kHz to 5 MHz. The frequency dispersion in the inversion regime, that is typical of minority carrier, is clearly visible for positive biases beyond +1 V. The capacitance for negative biases takes a single value, which is indicative of the accumulation regime. In-between these two points can be noticed a so-called C-V *bump*, in the regime corresponding to depletion. This *bump* shows a frequency dispersion, albeit a little less pronounced than in the inversion

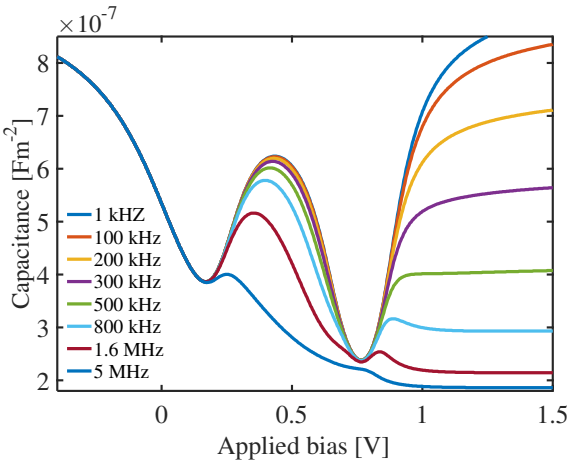


Figure 6.1: Frequency dispersion of C-V characteristics as a function of applied bias, both in the *bump* and in the inversion regime. Parameters for the simulation are listed in Tab. 6.1.

regime. It is attributed to the presence of the interface traps, as will be shown below.

Several physical parameters can be readily extracted from such a C-V characteristic [111]. To begin with, the capacitance in high accumulation is equal to the oxide capacitance C_{ox}. This allows to estimate its thickness when the dielectric constant of the material is known, or to confirm the value of that dielectric constant if the thickness is measured, *e.g.* by TEM (Transmission Electron Microscopy). The width of the depletion region W_d can then be determined. The total capacitance at high frequency C_{hf} for biases beyond the flatband potential V_{fb} is indeed the series combination of the oxide capacitance and the depletion capacitance C_s, which reads

$$C_{\text{hf}} = \left(\frac{1}{C_{\text{ox}}} + \frac{1}{C_d}\right)^{-1} \Leftrightarrow C_d = \left(\frac{1}{C_{\text{hf}}} - \frac{1}{C_{\text{ox}}}\right)^{-1}. \tag{6.1}$$

because neither the interface traps nor the minority carriers from inversion impact the C-V characteristics at sufficiently high frequency.

The depletion width is therefore extracted in a similar way as for a one-sided pn junction

$$W_d = \frac{\epsilon_s \epsilon_0 A}{C_d} = \epsilon_s \epsilon_0 A \left(\frac{1}{C_{\text{hf}}} - \frac{1}{C_{\text{ox}}}\right) \tag{6.2}$$

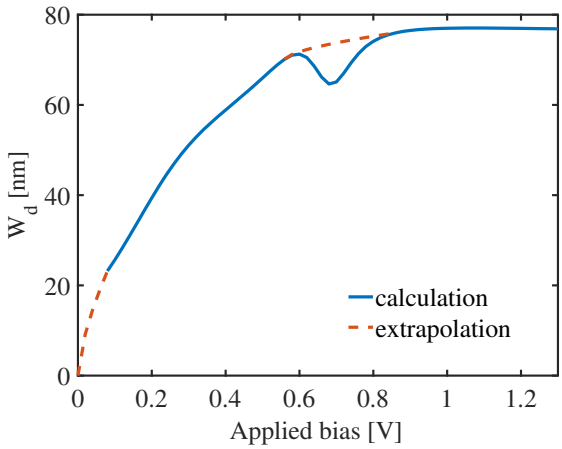


Figure 6.2: Depletion width W_d as a function of applied bias (full line) , extrapolated towards the flatband potential and around potentials corresponding to the *bump* in the C-V characteristics (dashed line).

Figure 6.2 shows the depletion width W_d as a function of applied bias, calculated from Eq. (6.2) and the 1 MHz C-V curve from Fig. 6.1. The full line curve reveals a small lessening between 0.6 V and 0.8 V, which is related to the little bump from the C-V that is actually still partially present even at high frequency. The curve is therefore extrapolated over that region (dashed line), and it is also extrapolated towards the flatband potential, where depletion is not deep enough to successfully apply the relationship, yet.

The depletion width increases with the applied bias in the depletion regime, then in the weak and strong inversion regimes where the maximum value is reached and the depletion width reaches a maximum value. This depletion capacitance is also directly linked to the bulk majority carrier concentration through the same relationship as the one linking the capacitance and carrier concentrations in pn junctions. In this case, though, the metal side is regarded as a material whose doping concentration tends to infinity, and the relation for $p \approx N_A$ reduces to

$$W_d = \sqrt{\frac{2\epsilon_s \epsilon_0 \phi_s}{qN_A}} \tag{6.3}$$

where $\phi_s = V - V_{\text{ox}}$ is the surface potential, accounting for the potential loss V_{ox} across the oxide from the total applied bias V. A similar relationship

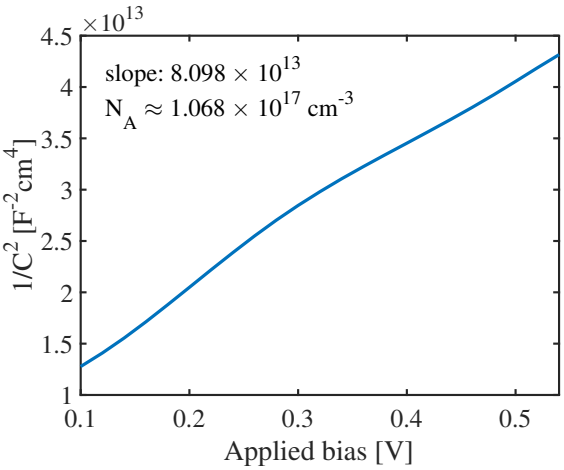


Figure 6.3: $1/C^2$ as a function of applied bias, whose slope is used to estimate the carrier concentration to 1.068×10^{17} cm^{-3}.

between $1/C^2$ and the carrier concentration can be established as for a pn junction [205]:

$$\begin{aligned} C &= \frac{\mathrm{d}Q}{\mathrm{dV}} = \frac{\mathrm{d}Q_s}{\mathrm{d}\phi_\mathrm{s}} = \frac{\mathrm{d}}{\mathrm{d}\phi_s}\left(-qN_A W_d\right) = \sqrt{\frac{qN_A\epsilon_s\epsilon_0}{2\phi_s}} \\ &\rightarrow \frac{\mathrm{d}(1/C^2)}{\mathrm{d}\phi_s} = \frac{\mathrm{d}(1/C^2)}{\mathrm{d}V} = \frac{2}{qN_A\epsilon_s\epsilon_0} \end{aligned} \tag{6.4}$$

where $Q_s = Q_d$ is the total charge in the semiconductor, which is mostly equal to the space charge in the depletion region under these conditions and in the absence of traps.

Figure 6.3 shows the corresponding $1/C^2$ curve, with a positive slope indicating the p-type doping of the semiconductor. The value of the slope allows to retrieve the input carrier concentration.

Oxide thickness

Figure 6.4 shows C-V characteristics of the MOS structure for three different oxide thicknesses: 10 nm, 20 nm and 30 nm. The oxide thickness has a direct effect on the geometric capacitance $C_{\mathrm{ox}} = \epsilon A/t_{\mathrm{ox}}$, which is visible in accumulation and in the strong inversion regime at low frequency (Fig. 6.4 (a)). The global capacitance values result from the series combination of

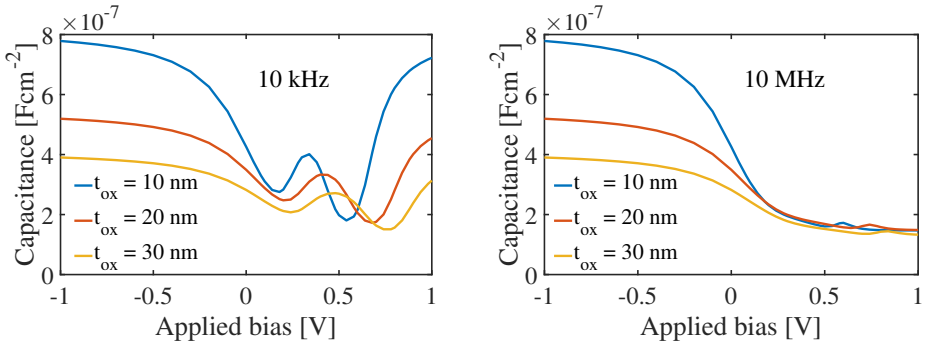


Figure 6.4: C-V characteristics as a function of applied bias for three different oxide thicknesses: 10 nm, 20 nm and 30 nm and two frequencies: (a) 10 kHz and (b) 10 MHz.

the oxide capacitance C_{ox} and the equivalent semiconductor capacitance C_s (originating from the depletion layer, the traps or the inversion layer). A thicker oxide therefore impacts the C-V characteristics such that the overall values are lower. The low frequency curve is flattened and spreads out horizontally for a thicker oxide layer, too. The flatband potential V_{fb} is not altered, although the inversion occurs more rapidly. This all comes from the spreading of the applied potential V over the larger oxide layer. Because of the continuity of the electric displacement field, the potential drop actually applied over the semiconductor boundaries is therefore lower for a given total bias V when the oxide thickness t_{ox} is larger.

Any displacement away from V_{fb} is slowed down and accumulation or inversion occur for larger applied biases. This is therefore also the case for the interface traps, whose *bumps* are shifted to higher bias and spread out horizontally for the thicker oxide thickness. At high frequency, the general characteristic is dominantly resulting from the depletion capacitance. As it is much smaller than the oxide capacitance, the series combination of the two overshadows the oxide capacitance. The impact of its variation is therefore limited to the value of the accumulation capacitance. As a consequence of these observations, it can be concluded that although an increase of the oxide thickness spreads out the C-V characteristics horizontally, it does not impact the position of V_{fb} or typical features other than the accumulation capacitance and the inversion capacitance at low frequency.

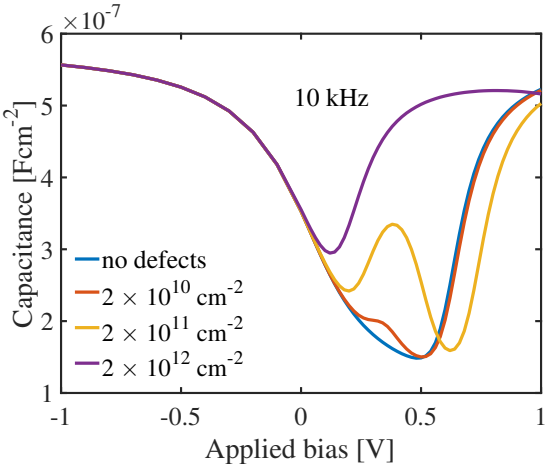


Figure 6.5: C-V characteristics as a function of applied bias for three different interface trap densities: 2×10^{10} cm^{-2}, 2×10^{11} cm^{-2} and 2×10^{12} cm^{-2} as well as in the absence of traps, at a frequency of 10 kHz.

6.2.1 Interface trap density and energy position

The density of interface traps, D_{it}, has a direct impact on the C-V *bumps* previously observed. Figure 6.5 shows the C-V characteristics at 10 kHz of three different interface traps densities: 2×10^{10} cm^{-2}, 2×10^{11} cm^{-2} and 2×10^{12} cm^{-2}. C-V characteristics in the absence of interface trap are also displayed for comparison. The large difference in height of the C-V *bumps* for $D_{it} = 2 \times 10^{10}$ cm^{-2} and $D_{it} = 2 \times 10^{11}$ cm^{-2} is clearly visible. For even larger densities, $D_{it} = 2 \times 10^{12}$ cm^{-2}, the resulting characteristics could be mistaken for a perfect capacitance response, in the absence of interface traps, unless it can be directly compared with curves simulated in the absence of traps, which are clearly different. The strong symmetry of the curve with large D_{it}, the value of the minimum and its position too close to the flatband potential also give it away as being the result of non-ideal conditions. Caution must therefore be exerted when interpreting a single C-V characteristic. The analysis carried out hereafter supports in a more extensive way the need for a cautious approach.

The C-V *bumps* related to the interface traps are also dependent on the energy positions of those traps. Figure 6.6 shows the low frequency (1 kHz) C-V characteristics for three different interface trap energy positions, located 120 meV, 240 meV and 360 meV above the valence band energy. The

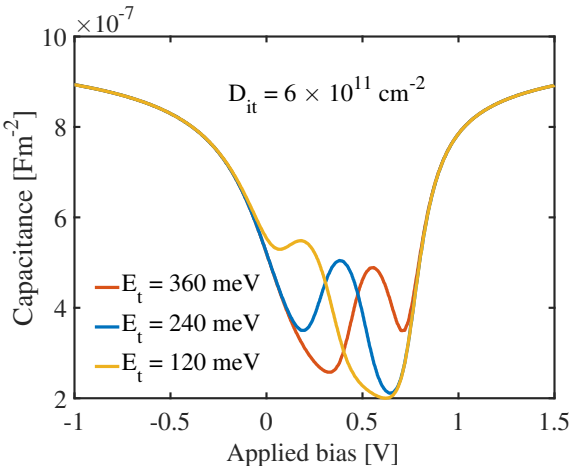


Figure 6.6: Low frequency (1 kHz) C–V characteristics for different interface traps energy positions E_t relative to the valence band energy and an interface trap density of 6×10^{11} cm^{-2}.

electronic trap states considered are acceptor types, which means that they do not contribute to the charge when they are empty. This is the case when the Fermi level is far below them. On the other side, if the Fermi level is much higher than the trap energy, it will be completely filled and act more as a dopant than a trap. The capacitance signal from the traps, that gives rise to the *bumps*, only occurs when the Fermi level E_F is close to the trap energy level E_t. Under that condition, the ac modulation of the Fermi level will modify the occupancy of the traps. The change in stored charge will therefore result in a capacitance signal, as per the definition of the small-signal capacitance $C = dQ/dV$. The maximum capacitance signal appears for the condition $E_F = E_t$.

This direct relation between the traps energy and the position of the C-V *bumps* is shown in Fig. 6.6. As the traps are located further away from the valence band, the *bump* positions are shifted to more positive biases. This is related to the applied bias required to reach the condition $E_F = E_t$, which occurs in the deeper depletion regime, or even towards the weak and strong inversion regimes for traps located above the others in the bandgap.

Trapped charges in the oxide

As previously observed, the oxide thickness does not influence the flatband potential. This is the case when a perfect oxide is assumed. The effect of

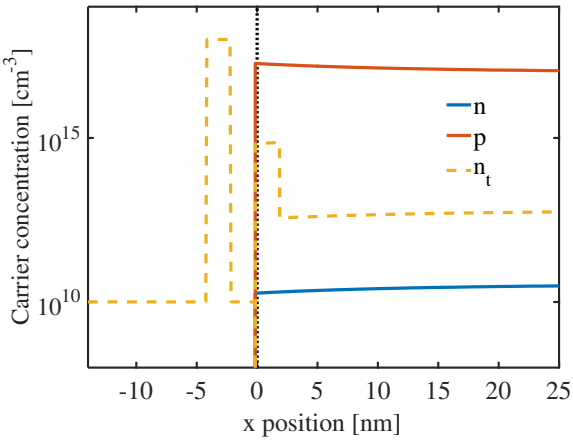


Figure 6.7: Microscopic carrier concentrations at the interface between the oxide and the semiconductor.

trapped charges in the oxide layer is analyzed here. We now consider electronic trap states located 2 nm from the interface, over a length of 2 nm as well (see Fig. 6.7 for the microscopic charge concentrations). The introduction of such traps in the oxide does not change anything to the situation concerning the leakage of current through the oxide. The numerical model in use does not include any conduction through the traps and as there are no free charges in the modeled oxide, conduction still cannot happen. These traps, located in the oxide layer, are able to generate fixed charges only.

When they are filled, they induce a fixed charge in the oxide

$$Q_{ox} = -qN_t^{\mathrm{ox}} d_t^{\mathrm{ox}} \simeq -3.2 \times 10^{-8}\,\mathrm{C}/cm^2 \tag{6.5}$$

which results in a potential shift $\Delta V = Q_{\mathrm{ox}}/C_Q$ where $C_Q = \epsilon_{\mathrm{ox}}\epsilon_0 A/d_{\mathrm{ox}}$ is the geometric capacitance due to the distance d_{ox} between the charges and the gate contact. In our case, with an average distance of $d_{ox} = 12.5$ nm, the value of this capacitance would be $C_Q \simeq 6.59 \times 10^{-7}$ F/cm^{-2}. The flatband potential V_{fb} is therefore altered as

$$V_{fb+Q_{ox}} = V_{fb} - \frac{Q_{\mathrm{ox}}}{C_Q} \approx 0.05\,\mathrm{V}. \tag{6.6}$$

Figure 6.8 shows the C-V characteristics with and without fixed traps in the oxide, which indicate that the flatband potential shift is similar to

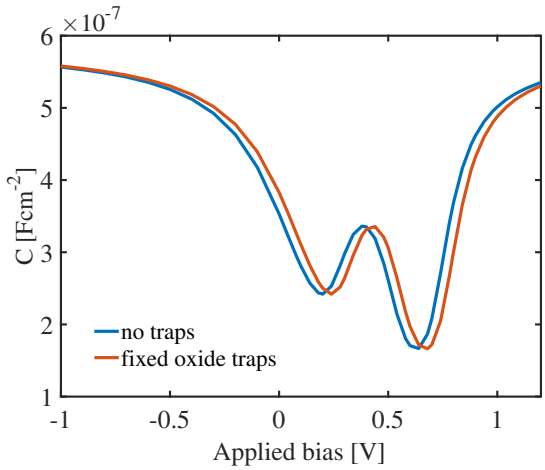


Figure 6.8: C-V characteristics without traps and with a 10^{18} cm^{-3} concentration of fixed traps in the oxide.

the calculated shift. No effect is observed, though, on the *bump*'s height or position, beyond that of the V_{fb} shift.

In structures containing fixed charges in the oxide like these, a shift in the value of V_{fb} is therefore expected. Moreover, a variation of the oxide thickness will now incur a flatband potential shift, because the capacitance associated with the fixed charges will change together with their distance from the gate surface.

6.2.2 Effect of temperature

The temperature is expected to impact both the response of the traps and the response of the minority carriers. We therefore performed simulations for temperatures ranging from $T = 300$ K down to $T = 100$ K.

Figures 6.9 (a) to (d) show the influence of the temperature on the C-V characteristics at four frequencies: 10 kHz, 100 kHz, 1 MHz and 10 MHz. The impact of temperature on the minority carriers is clearly visible in the high frequency characteristics. Although the higher temperature curves for 300, 290 and 270 K were are distinguishable at 10 kHz, they become discernable at the 100 kHz or the1 MHz frequency. This confirms that the cut-off frequency of the minority carriers decreases with the temperature. As the numerical model does not include a variation of the mobility with the temperature, this effect is only related to the temperature dependence of the band-to-band recombination rate of minority carriers.

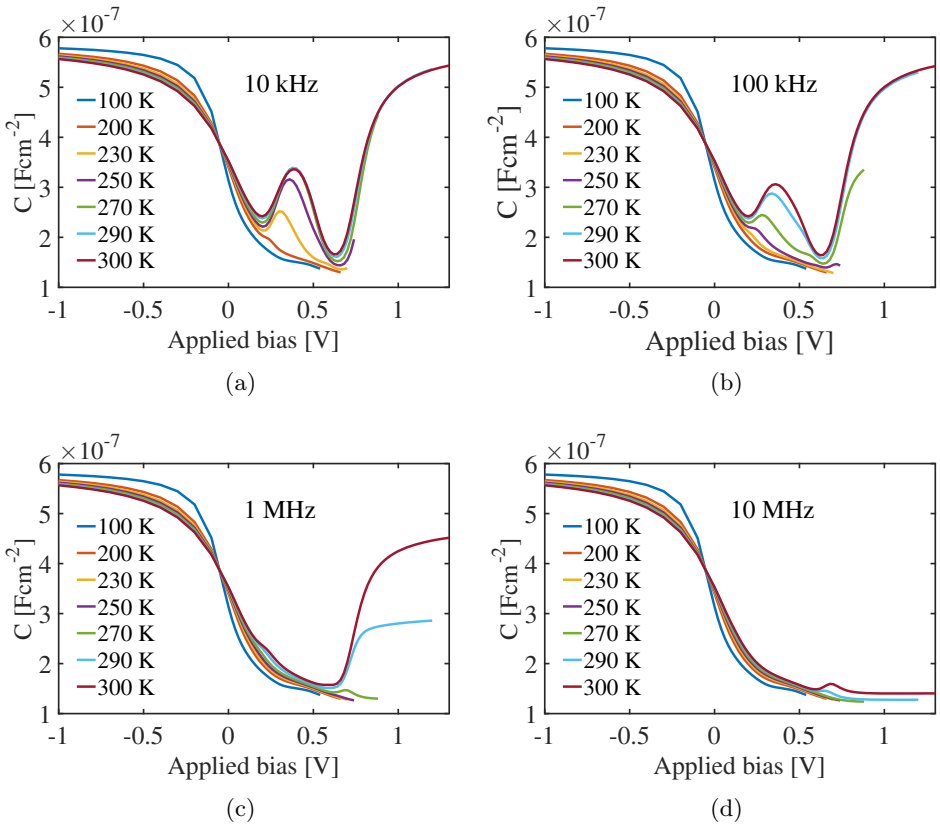


Figure 6.9: C-V characteristics as functions of applied bias for temperatures between 100 K and 300 K and frequencies from 10 kHz to 10 MHz.

Similarly, frequency dispersion in the *bump* occurs for lower frequencies at lower temperatures, too. This is related to the temperature dependence of the trap emission rate

$$e_p = \sigma_p \, v_p^{th} \, N_v \, \mathrm{e}^{-\dfrac{E_t - E_V}{kT}} \propto \mathrm{e}^{-1/T} \tag{6.7}$$

In accumulation, the main difference with the other curves can be observed for the $T = 100$ K curve, which has a larger accumulation capacitance. This likely originates from a faster transition between the depletion and accumulation regimes at this low temperature. The other accumulation curves have not yet reached the oxide capacitance (588 nF/cm^2) and would need a larger negative bias to do so. This enhanced transition at low temperature results from the lower carrier concentration because of the temperature dependence of the Maxwell-Boltzmann statistics, which carries a mostly exponential behaviour as well [111]:

$$p = 2 \left(\frac{2\pi m_h^* kT}{h^2} \right)^{3/2} \mathrm{e}^{-\dfrac{E_F - E_V}{kT}} \propto \mathrm{e}^{-1/T} \tag{6.8}$$

6.3 The conductance method

In this Section, the characterization of interface traps with the conductance method will be investigated. Indeed, it is difficult to extract quantitative information from C-V characteristics in the presence of traps without the knowledge of other parameter values such as, *e.g.*, the oxide thickness. The conductance method has no such limitations, but the information extracted from this technique can suffer from other side effects, such as in particular the inversion response. The effect of energy position and extension within the bandgap has therefore been assessed.

The general principles of the conductance method have been developed in Subsection 3.4.2 from Chapter 3 (page 21). They are based on the measurement of the parallel conductance G_p as a function of angular frequency ω. For each bias applied to the MOS structure, the curve of $G_p(\omega)/\omega$ shows a maximum for a given frequency. The value of that maximum, $(G_p/\omega)_{\max}$, is directly linked to the interface state density at the energy corresponding to the position of the Fermi level for that bias. Figure 6.10 shows a 2D mapping of $G_p(\omega)/\omega$ as a function of frequency and applied bias for interface traps located 200 meV above the valence band energy. For each bias value, there is a maximum in the curve of $G_p(\omega)/\omega$ as a function of frequency. For

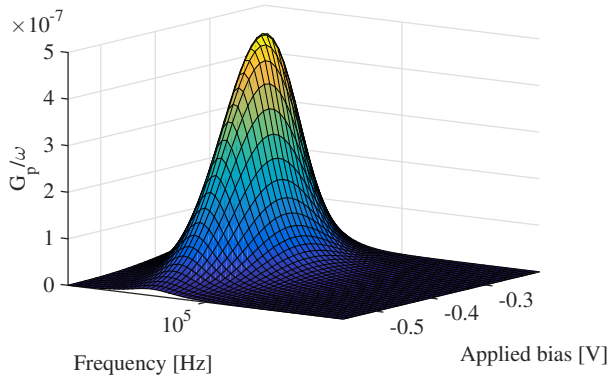


Figure 6.10: Two-dimensional mapping of the parallel conductance (G_p/ω) as a function of frequency and applied bias for interface traps located 200 meV above the valence band energy.

a given bias, the peak value of $G_p(\omega)/\omega$ is higher than all others. This peak value will later be shown to correspond to a Fermi level energy of 200 meV and, according to the theory of the conductance method [127], its height is directly related to the trap density of 6×10^{11} cm^{-2}.

In order to first further illustrate the method and get a better feeling of its operation, qualitative parallel conductance mappings with a few different interface traps situations are displayed in Fig. 6.11. The first column, Fig. 6.11 (a), (c) and (e), shows the impact of the trap energy position in the bandgap. The trap energy extensions are constant and relatively narrow, with $\Delta E_t = 10$ meV and three energy positions are represented: (a) 300 meV, (c) 250 meV band and (e) 200 meV above the valence band. On those maps, a yellow region of high G_p/ω values can be observed, corresponding to the peak conductance response of the traps. This peak maintains a similar shape over all three maps, but it is shifted both as a function applied bias and frequency when the trap energy position is modified. This illustrates clearly the theoretical relationship between peak frequency and the energy position: as the traps are located further away from the valence band, their peak frequency is reduced. This frequency dependence will be further discussed in Subsection 6.3.3, devoted to the interface traps time constant. The relationship with the applied bias is also readily explained: when the traps are located lower in the bandgap, the bias corresponding to the maximum G_p/ω values is low, because the Fermi level required to probe the traps is also low, then. Conversely, for traps located farther away from

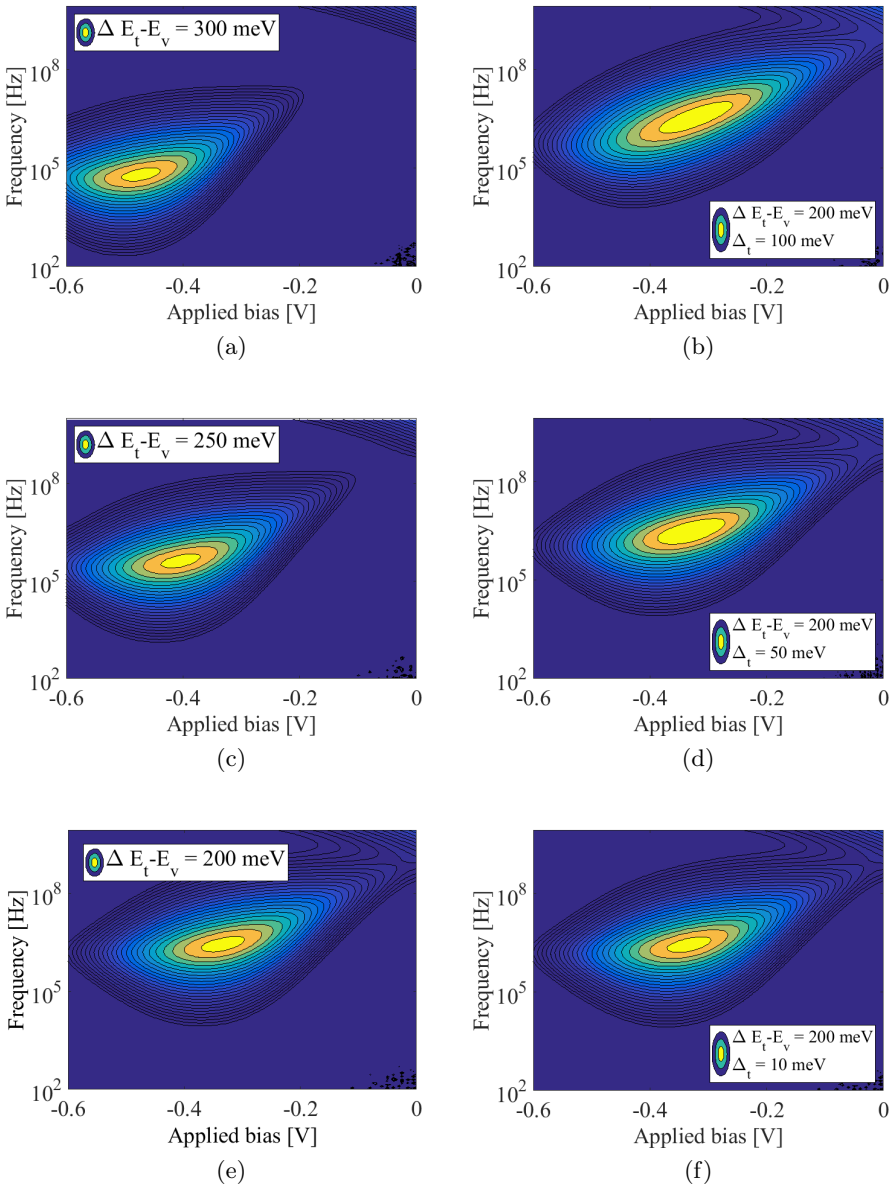


Figure 6.11: 2D map of the conductance G_p/ω as a function of both the frequency and applied bias V, for trap energy extensions $\Delta E_t =$ 10 meV and (a) $E_t - E_v = 300$ meV, (c) $E_t - E_v = 250$ meV, (e) $E_t - E_v = 200$ meV, and for $E_t - E_v = 200$ meV and energy extensions (b) $\Delta E_t = 100$ meV, (b) $\Delta E_t = 50$ meV and (f) $\Delta E_t = 10$ meV.

the valence band, a higher bias is necessary to move the Fermi level up to the traps energy level, where it is able to modulate their occupancy.

In the second column of Fig. 6.11, the trap energy position is fixed and centered around 200 meV above the valence band. It is now the extension of the traps energy distribution that is varied from (b) $\Delta E_t = 100$ meV to (d) $\Delta E_t = 50$ meV and finally (f) $\Delta E_t = 10$ meV. As the energy position of these traps is constant, the centers of the regions of high G_p/ω values remain at the same location, both in terms of frequency and applied bias, for all three cases. The only visible variation affects the shape of the regions of maximum values. These regions spread out as the energy distribution enlarge, with the yellow region in map (b) ($\Delta E_t = 100$ meV) being much more widespread than in map (f), corresponding to the thinner distribution ($\Delta E_t = 10$ meV).

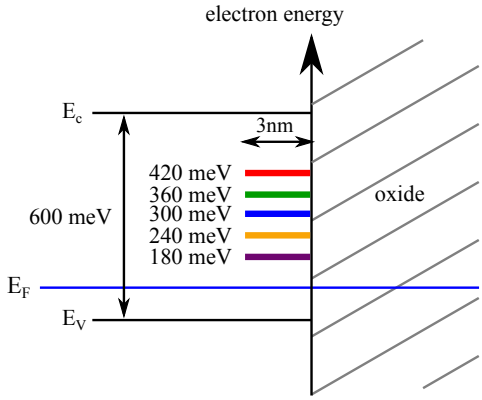


Figure 6.12: Schematic of the interface states with energies from 180 meV to 420 meV above the valence band energy.

6.3.1 Discrete energy levels

Discrete trap energy levels have first been investigated with the conductance method. These traps are modeled as a thin (3 nm) layer on the semiconductor side of the interface. The traps energy states extend over 6 meV within the bandgap (which is about 1% of the bandgap size) so as to obtain quasi-discrete energy levels.

The effect of the energy position of the traps is evaluated, with traps located at various energy positions within the bandgap. The traps have an energy distance from the valence band ΔE_t comprised between 180 meV

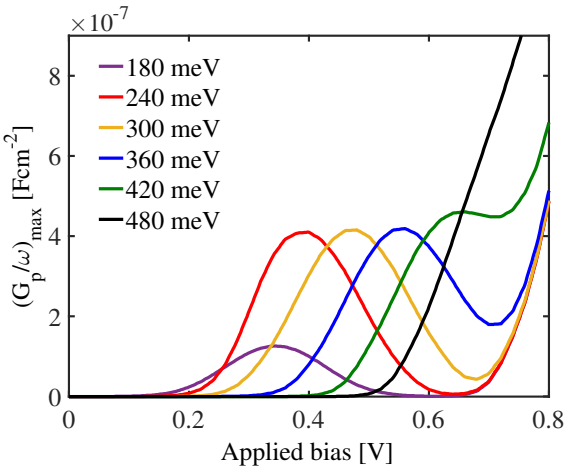


Figure 6.13: $(G_p/\omega)_{\max}$ (with respect to the frequency) plotted as a function of applied steady state bias for various energy positions within the bandgap and two different interface state densities.

and 480 meV, as schematically represented in Fig. 6.12. An interface trap density $D_{it} = 6 \times 10^{11}$ cm^{-2} is considered. From the numerical simulation of the complete conductance response, the maximum value of G_p/ω as a function of frequency is selected and this $(G_p/\omega)_{\max}$ value is plotted as a function of applied bias in Fig. 6.13. The results show that for each trap energy position, the applied bias for which the maximum of $(G_p/\omega)_{\max}$ is reached shifts towards more positive values with $E_t - E_v$. This directly derives from the value of the Fermi level required to probe each trap energy, which requires increasingly high dc biases to be reached.

Comparing with the simulated Fermi level resulting from each applied bias confirms that the maximum of $(G_p/\omega)_{\max}$ is systematically obtained for a bias value that corresponds to a Fermi level equal to the trap energy level. Using the relationship giving the interface trap density D_{it} as a function of $(G_p/\omega)_{\max}$,

$$D_{it} = K\frac{(G_p/\omega)_{\max}}{Aq}$$

where A is the section area and K is an empirical value which we fitted to the data, the input interface trap density can be recovered from the height of the $(G_p/\omega)_{\max}$ peaks.

The applicability of the relationship is confirmed only for interface trap

energies close to the middle of the gap energy, though, *i.e.* between $E_t - E_v = 240$ meV and $E_t - E_v = 420$ meV. For biases starting from $E_t - E_v = 420$ meV, the conductance response increases strongly, regardless of the trap concentration or energy. For those trap energies, the conductance response is dominated by the inversion response. This response originates from the transitions between the trap states and the conduction and valence bands, and starts to occur for biases corresponding to those trap energies. The traps whose energy position requires such dc biases are therefore not accessible through the conductance method. This is obviously the case for the $E_t - E_v = 480$ meV energy level in Fig 6.13, as there is even no peak value anymore.

Traps that are too close to the valence band, on the other hand, cannot be detected either. This is the case for the $E_t - E_v = 180$ meV trap level. The initial Fermi level position at 0 V is indeed such that those traps are already at least partially activated. The oscillations of the Fermi level therefore cannot modulate those traps occupancy to their maximum, and the direct relationship between the $(G_p/\omega)_{\max}$ and D_{it} values is lost.

These findings already demonstrate the limitations that occur in the extraction of D_{it} with the conductance method. The impact of the inversion response is particularly strong, as it can restrain not only a correct extraction of the D_{it}, but also prevent the mere detection of the corresponding traps.

The influence of the actual D_{it} value is subsequently gauged. Densities in a 1 : 2 ratio are used, namely 6×10^{11} cm^{-2} and 1.2×10^{12} cm^{-2}. Figure 6.14 shows the immediate effect of those two different interface trap densities on the conductance. It is obvious that the height of the $(G_p/\omega)_{\max}$ peaks scales proportionally when the interface trap density is doubled. For a given trap energy position $E_t - E_v$, the bias corresponding to the peaks is shifted to more positive values when the D_{it} increases, though. The origin of this shift resides in the movement of the Fermi level with the applied bias, which moves more slowly towards the top of the bandgap interface when the trap density is increased.

The actual Fermi level corresponding to a given applied bias is part of the microscopic quantities provided by the simulations. The effect of the interface traps positions on the connection between the applied bias and the actual Fermi level can accordingly be characterized. Figure 6.15 shows that, although the $E_F - V$ relationship is initially linear, the presence of traps at a certain energy level induces a lag in the evolution of the interface Fermi level as a function of the applied bias. This lag occurs at small biases for

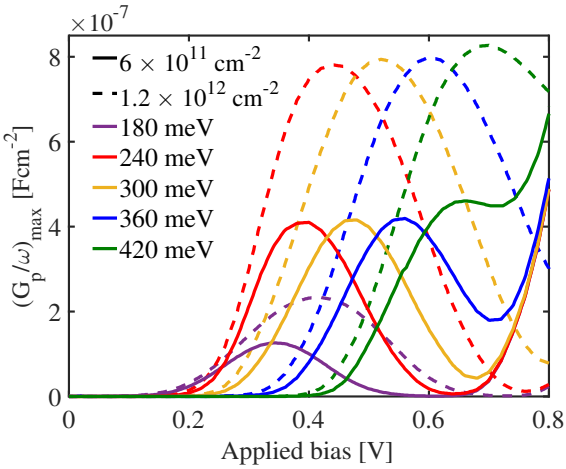


Figure 6.14: $(G_p/\omega)_{\max}$ (with respect to the frequency) plotted as a function of applied steady state bias for various energy positions within the bandgap and two different interface state densities: 6×10^{11} cm^{-2} (full lines) and 1.2×10^{12} cm^{-2} (dashed lines).

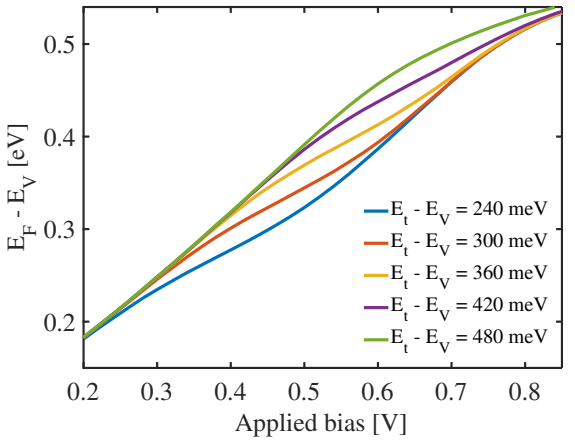


Figure 6.15: Fermi level position with respect to the valence band edge at the GeSn/oxide interface as a function of applied bias for discrete energy traps located at various positions in the bandgap.

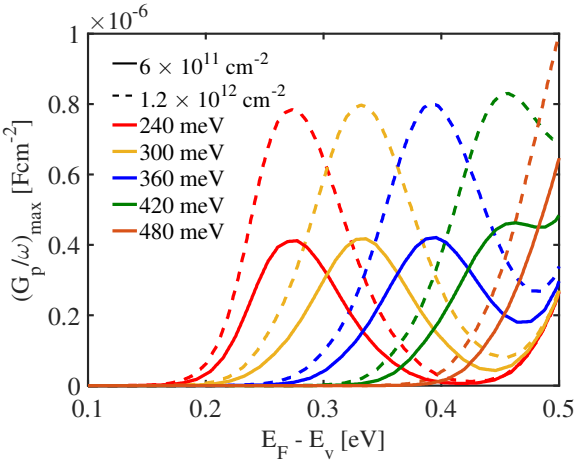


Figure 6.16: $(G_p/\omega)_{\max}$ (with respect to the frequency) plotted as a function of Fermi level at the interface (corresponding to the biases applied in Fig. 6.14) for various energy positions within the bandgap and two different interface state densities.

$E_t - E_v = 240$ meV, whereas it starts to occur at biases larger than ~ 0.6 V for $E_t - E_v = 480$ meV. This confirms that the lag of the Fermi level is directly related to the presence of the traps. Indeed, as the Fermi level crosses a trap level, those traps get filled with electrons and the Fermi level is maintained at that value until they are completely loaded with electrons. This effect is, of course, intensified by the D_{it} value. As there are more traps to be filled, the lag of the Fermi level is even more pronounced.

In order to clarify this effect on the peaks positions of the conductance method, the same $(G_p/\omega)_{\max}$ curves as in Fig. 6.14 have been plotted again. This time, though, they are displayed as a function of the interface Fermi level obtained from the data of Fig. 6.15. Figure 6.16 shows that the peaks corresponding to the same trap energies but different D_{it} values are now located at an identical x-position. This confirms that the shift previously observed in Fig. 6.14 for two interface trap densities and a same trap energy level was due to the hindering of the Fermi level displacement, resulting from the charging of the interface traps.

These results indicate that the energy position of the traps cannot be immediately deduced from the applied bias, as this position with respect to the bias depends on the density of those traps. The energy position of the detected traps must therefore be determined in another way, namely as a

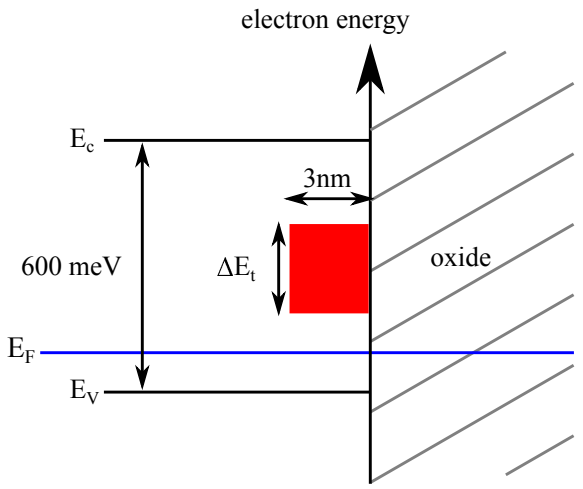


Figure 6.17: Schematic of the interface states with energies extending over an increased energy range ΔE_t, centered around the mid-gap energy.

function of the conductance response peak frequency.

6.3.2 Extended energy distributions

Traps in real devices are not always located at discrete energy positions in the bandgap, so we also investigated interface traps with more widespread energy ranges. Those traps possess the same spatial extension on the semiconductor side of 3 nm, as before. Their energy extension ΔE_t, though, now increases from 6 meV to 180 meV, as schematically represented in Fig. 6.17. In order to isolate the effect of the traps energy extension, the trap distribution is centered around the mid-gap energy, 300 meV above the valence band, for all cases. The narrowest distribution extends over $\Delta E_t = 6$ meV, which corresponds to trap spread out from 297 meV to 303 meV above the valence band. The widest distribution of traps is $\Delta E_t = 180$ meV, in which case the traps extend from 210 meV to 390 meV above the valence band.

Figure 6.18 shows the $(G_p/\omega)_{\max}$ curves of the conductance method as a function interface Fermi level energy for these increasingly widespread trap energy distributions. The width of the $(G_p/\omega)_{\max}$ peaks is broadened, indicating that the interface traps are distributed at energies gradually farther from the middle of the bandgap. The maximum values of $(G_p/\omega)_{\max}$ as a function of Fermi level energy, though, remain at the same position for all

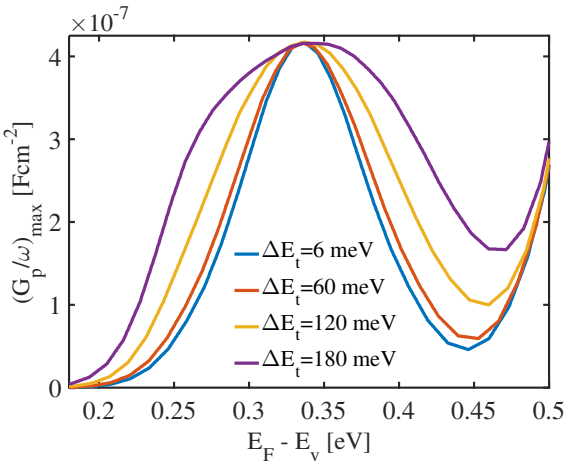


Figure 6.18: $(G_p/\omega)_{\max}$ (with respect to the frequency) plotted as a function of Fermi level at the interface for trap energies centered around the middle of the bandgap and increasingly widespread energy distributions.

trap distributions. Identical interface traps concentrations do not result in the same $(G_p/\omega)_{\max}$ values for all energy extensions, though. Different interface traps densities have therefore been used, so that they lead to identical $(G_p/\omega)_{\max}$ values, for the clearness of Fig. 6.18.

The values of $(G_p/\omega)_{\max}$ for a constant interface trap concentration indeed vary slightly with the energy extension. Figure 6.19 shows the relative variation of the $(G_p/\omega)_{\max}$ values as a function of trap energy extension, as compared to the narrowest distribution of 6 meV. The difference can be as high as 80% for the widest distribution, $\Delta E_t = 180$ meV as compared to the thinnest extension, $\Delta E_t = 6$ meV. This observation indicates another limitation on the accuracy of the extracted D_{it} value, as a unique K parameter cannot be used for all trap energy distributions.

In order to evaluate whether a direct relationship between the D_{it} value and the conductance response can still be found with traps extending over a wide energy range, we consequently simulated the conductance response of interface traps with an intermediate extension of 120 meV within the bandgap. As before, various energy positions within the bandgap are considered. The same shift in the applied bias versus interface Fermi level as in Fig. 6.14 was obviously still present, so we directly plotted the values of $(G_p/\omega)_{\max}$ as a function of interface Fermi level in Figure 6.20. Two dif-

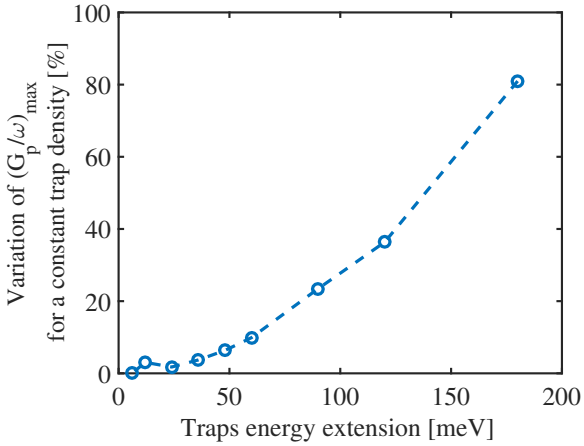


Figure 6.19: Relative variation of the value of $(G_p/\omega)_{\max}$ (with respect to the frequency) plotted as a function of the interface trap energy extension for a constant interface trap density, compared to the value of $(G_p/\omega)_{\max}$ for the thinnest extension, 6 meV.

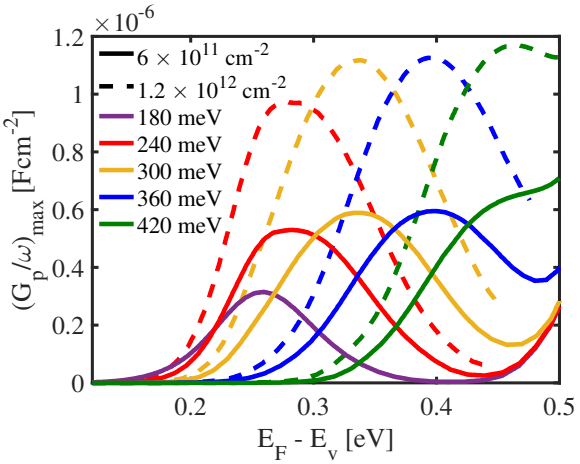


Figure 6.20: $(G_p/\omega)_{\max}$ (with respect to the frequency) plotted as a function of Fermi level at the interface for trap energies extending over a range of 120 meV, different positions in the bandgap and two trap densities.

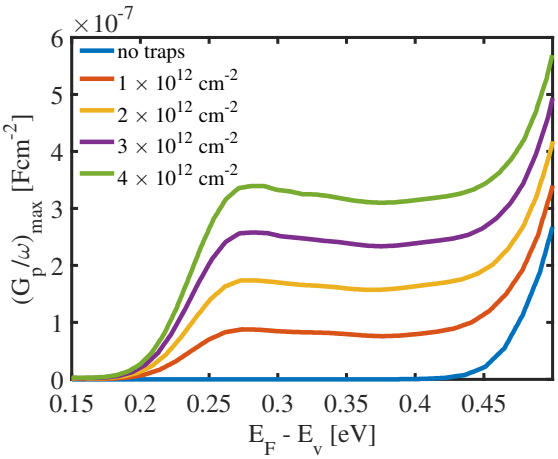


Figure 6.21: $(G_p/\omega)_{\max}$ (as a function of frequency) plotted as a function of Fermi level at the interface for trap energies extending almost over the whole bandgap. Various trap densities are displayed.

ferent interface trap densities are displayed, with the dashed lines having the same trap energy position as the full lines, but with twice as large a concentration. In the same way as the quasi-discrete trap energies, the position of the maximum of $(G_p/\omega)_{\max}$ moves to higher Fermi energies when the traps get closer to the conduction band. The value of that maximum of $(G_p/\omega)_{\max}$ is also doubling when the interface trap densities are doubled, again indicating a direct relationship between the interface trap density D_{it} and the peak value of $(G_p/\omega)_{\max}$. The main difference is certainly the width of the peaks as a function of Fermi energy. As these traps are present over a larger energy range, the corresponding peak in the conductance response is accordingly wider. These results confirm that the D_{it} value extracted in the case of larger trap energy extensions remains proportional to the actual trap density, although a slightly different K factor is involved.

To complete this investigation, traps extending almost over the whole bandgap have been considered. Those are present from 6 meV above the valence band to 6 meV below the conduction band, thus covering 98% of the bandgap energy. Figure 6.21 shows the value of $(G_p/\omega)_{\max}$ as a function of Fermi level energy at the interface for various interface trap densities. The value of the maximum parallel conductance $(G_p/\omega)_{\max}$ is almost constant over a large Fermi energy range. That constant value is also increasing proportionally to the interface trap density, indicating that detection of in-

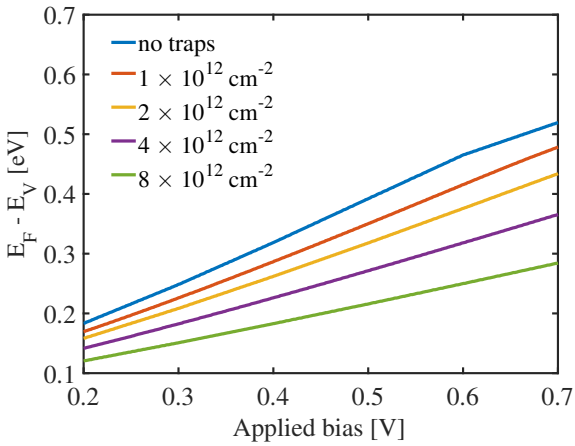


Figure 6.22: Fermi level at the GeSn/oxide interface as a function of applied bias for traps extending over the whole bandgap and various interface trap densities.

terface traps with the conductance method can still be performed in this case. Interface traps located close to the valence or conduction bands are again seen to be unattainable, though. Indeed, the curve corresponding to the absence of interface traps shows the same increase as the other curves towards Fermi energies close to the conduction band. This confirms that this response is not linked to the traps but to the conduction response at weak, and then high, inversion.

The curves shown in Fig. 6.21 are, again, directly plotted as a function of the interface Fermi energy. On the original curves as a function of applied bias, a shift towards higher bias for higher interface traps densities could indeed be observed. This shift originates from the dependence on the interface trap density of the relationship between the Fermi level and the applied bias. Figure 6.22 shows this relationship, where the Fermi level at the GeSn/oxide interface is plotted as a function of applied bias for various interface trap densities. This shows that for a given applied bias, the Fermi level is held back closer to the valence band when the interface trap density is higher. As opposed to the discrete energy traps, the lag of the Fermi level does not occur for a restricted range of biases. It occurs from the start, and the relationship between the applied bias and the Fermi level remains linear. The interface trap density impacts the slope of that relation, though, which is lower when the interface trap density is higher.

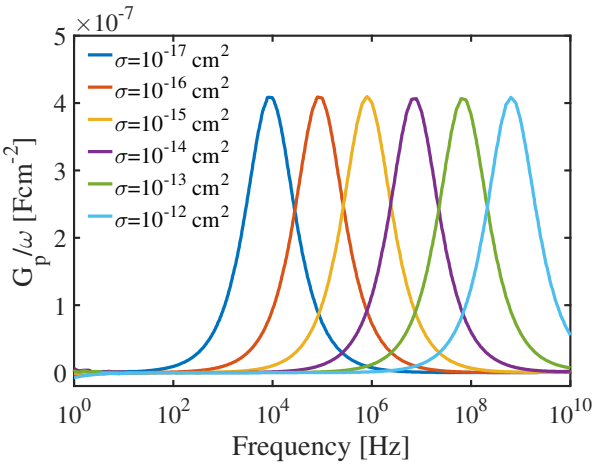


Figure 6.23: G_p/ω as a function of frequency for various interface traps cross sections σ and $D_{it} = 6 \times 10^{11}$ cm^{-2}.

In this section, we probed the application of the conductance method on low bandgap GeSn materials with various forms of interface traps. The most noticeable results are the strong impact of the inversion response and the variable relationship between the applied bias and interface Fermi level. The effect of the inversion response can, in some cases, totally impair the extraction of D_{it}. As for the relationship between the applied bias and the interface Fermi level, it varies widely with interface traps density and energy position, and therefore does not allow to accurately determine the trap energy position.

6.3.3 Interface traps time constant

The interface trap energy position can be estimated from their time constant, though, as is shown in this subsection. But first, for a trap to be accessible through the conductance method using the standard 100 Hz - 1 MHz frequency range, which is related to the practical instrumental constraints, the frequency f_{it} for which G_p/ω is maximum has to be in that range. This frequency f_{it} depends in particular on the capture cross section of the traps σ and on the energy difference with the majority carrier band edge ΔE [127]:

$$f_{it} = \left(v_{\text{th}}\, \sigma\, N_{\text{eff}}\, e^{(-q\Delta E/kT)} \right). \tag{6.9}$$

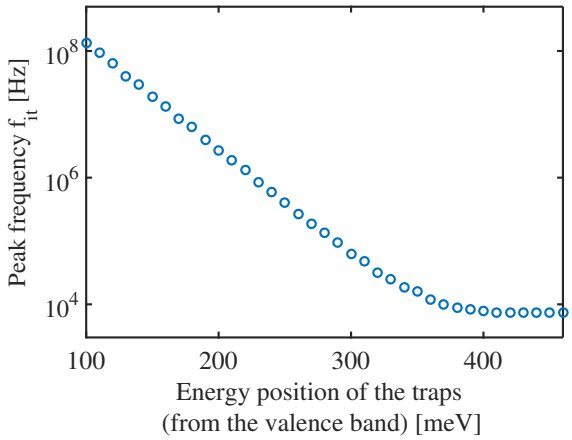


Figure 6.24: Evolution of the traps peak frequency f_{it} as a function of the trap energy position above the valence band ΔE, for 10 meV wide trap distributions.

Figure 6.23 shows G_p/ω curves as a function of frequency for various orders of magnitude of the capture cross section σ. For smaller capture cross sections, the frequency required to reach the peak value $(G_p/\omega)_{\max}$ increases. The linear relationship between the capture cross section and the peak frequency is also clearly observable in this Figure.

The peak frequency of G_p/ω can also be used to calculate the energy position of the traps from Eq. (6.9). Figure 6.24 shows the evolution of the peak frequency f_{it} with the energy position of the traps in the bandgap. These simulations indicate that the relationship remains exponential (linear in this logarithmic plot) up to traps located 350 meV above the valence band. For traps beyond 350 meV, their conductance response is overshadowed by the inversion response, anyway, so that neither their density nor energy position can be determined. In situations not affected by this inversion response, though, the simulations confirm that the relationship offers another way to estimate the energy position being probed in the bandgap, which is not directly accessible from the value of the applied potential.

The frequency f_{it} also depends on other parameters, such as the thermal velocity and the effective density of states. Those quantities, in turn, depend on the temperature, but this dependence is dwarfed by the direct exponential temperature dependence of the f_{it}. This dependence on the temperature offers a commonly used possibility to extend the detection range to traps

whose capture cross section or energy position make them unaccessible at room-temperature.

6.4 Inversion response of minority carriers

The previous Section revealed the major impact of the inversion response of minority carriers on the applicability of the conductance method. In the presence of a non-detected inversion response, the D_{it} value is overestimated. This section is therefore dedicated to the analysis of the inversion response dependence on material parameters such as the bandgap energy and the charge carriers effective masses and mobilities. These simulations support the interpretation of experimental C-V characteristics performed with high-k gate stacks on tensile strained Ge or tensile strained GeSn layers [204].

The C-V characteristics of the MOS structure for various bandgap energies comprised between $E_g = 0.4$ eV and $E_g = 0.8$ eV have therefore been investigated, in order to assess the impact of a low bandgap energy. For each of those bandgap energies, Fig. 6.25 (a) shows the 1 kHz frequency curve and Fig. 6.25 (b) shows a higher, 316 kHz, frequency curve.

The effect of the bandgap is clearly confirmed on the low frequency curve, as the inversion response occurs increasingly fast when the bandgap energy is smaller. The onset of the inversion response is shifted by as much as 0.12 V for each reduction of 100 meV of the bandgap energy.

At 316 kHz, frequency dispersion already occurs for the bandgap energies of 0.8 eV and 0.7 eV, partially for the 0.6 eV energy and not yet for the lower bandgap energies. This indicates that for lower bandgap energies, the minority carriers remain able to respond to the external bias for higher frequencies. As Fig. 6.25 (c) shows, the minority carriers are actually still responding at the 1 MHz frequency, which is typically the maximum frequency used in CMOS characterizations.

Figure 6.26 shows the effect of the electron and hole effective masses on the C-V characteristics at 1 kHz for a constant bandgap energy $E_g = 0.54$ eV. The impact on the onset of the inversion response, although not as critical as that of the bandgap energy, is visible. The reduction of the effective mass of electrons (minority carriers) clearly shifts the onset of the inversion response to higher potentials, whereas the effective mass of holes (majority carriers) alters its onset in the same way, but to an even much lesser extent. This dependence is directly related to the p-type doping of the semiconductor.

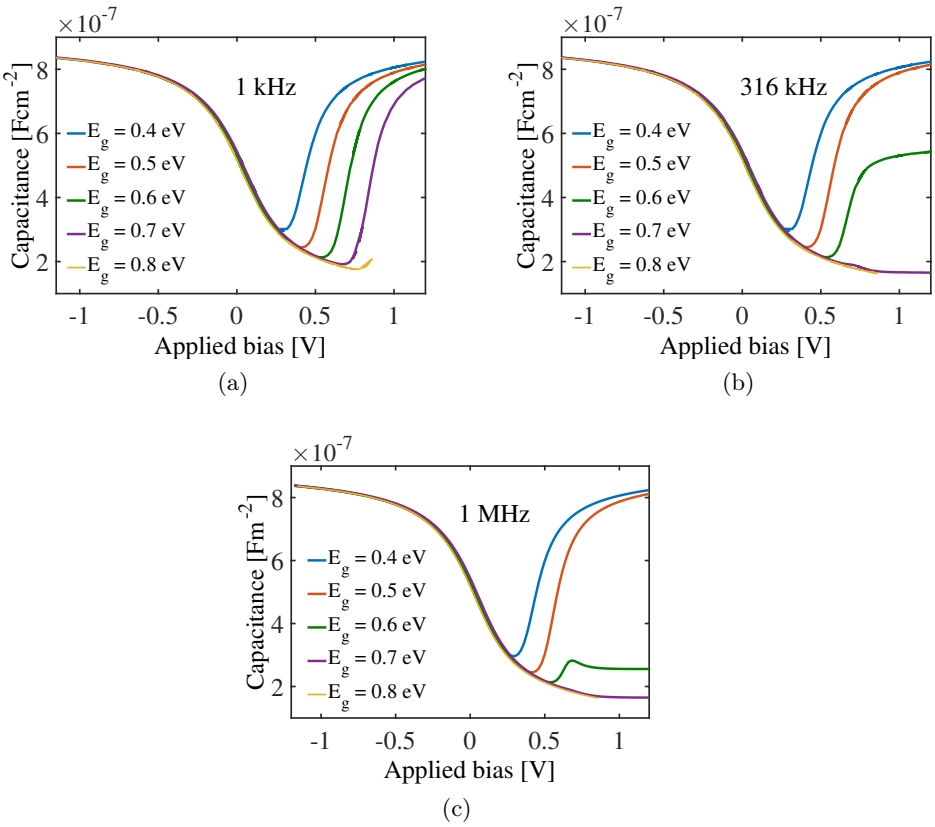


Figure 6.25: C-V characteristics of the MOS structure for various bandgap energies from $E_g = 0.4$ eV to $E_g = 0.8$ eV and (a) 1 kHz frequency, (b) 316 kHz frequency and (c) 1 MHz frequency.

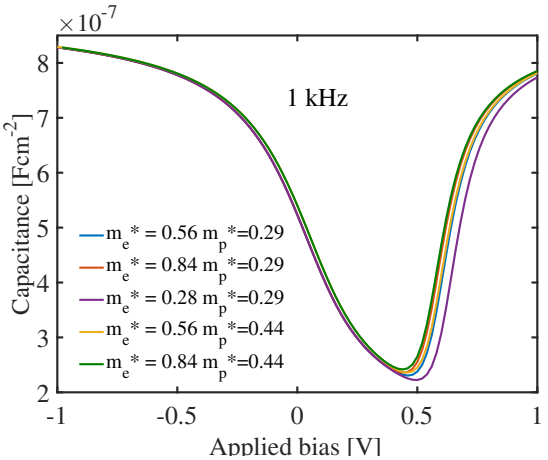


Figure 6.26: C-V characteristics of the MOS structure for various combinations of the electron and hole effective masses at 1 kHz and $E_g = 0.54$ eV.

Indeed, the inversion regime corresponds to an increase in the population of minority carriers, which are therefore electrons in this case.

The influence of both the majority and minority carriers mobilities has also been considered. Figure 6.27 shows the C-V characteristics at 1 MHz and a constant bandgap energy $E_g = 0.54$ eV for different combinations of hole mobility μ_p and electron mobility μ_n. The simulations indicate that the inversion responses increases with higher electron (minority carriers) mobility. The hole (majority carriers) has no impact on the inversion response.

6.4.1 High-k gate stacks

These observations allow to support the interpretation of experimental measurements performed in [204], where the challenges due to the very low bandgap with respect to the correct electrical characterization of Ge(Sn)/high-k MOS capacitors are highlighted.

Both strained Ge and strained GeSn layers with 6% Sn content are compared with a reference Ge virtual substrate (VS). Two strain levels, namely 1.1% and 1.4%, are considered for the Ge layer and 0.4% tensile strain is attained for the GeSn layer. Different high-k gate stacks are also deposited: 5 nm Al_2O_3, 1 nm Al_2O_3/4 nm HfO_2 or 5 nm HfO_2. Full details of the preparation of the samples are available in Ref. [204].

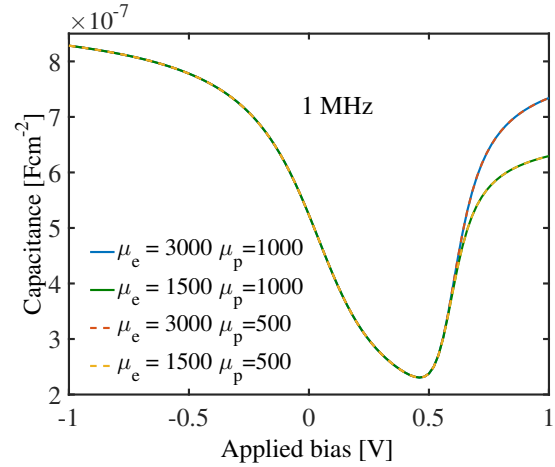


Figure 6.27: C-V characteristics of the MOS structure for various electron and hole mobilities at 1 MHz and $E_g = 0.54$ eV.

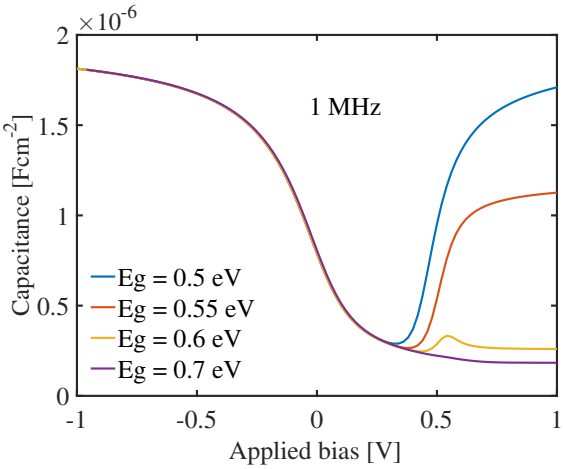


Figure 6.28: C-V characteristics of the MOS structure with a 5 nm Al_2O_3 gate oxide for various bandgap energies from $E_g = 0.5$ eV to $E_g = 0.7$ eV and 1 MHz frequency.

First, as already pointed out by the previous simulations and confirmed by the adapted simulation of a 5 nm Al_2O_3 gate oxide in Fig. 6.28, at small bandgaps, *e.g.* ~ 0.54 eV for the 1.4% tensile strained Ge, the inversion response is still very strong at high frequency (1 MHz). This can be the cause of severe imprecisions in the determination of the interface trap density D_{it}. Room-temperature C-V measurements have first been performed on the Ge-VS with the various gate stacks presented above, as shown in Fig. 6.29 (a). The highest capacitance in accumulation is obtained for the same oxide thickness of 5 nm and HfO_2, as expected from the higher dielectric constant, compared to Al_2O_3 and Al_2O_3/HfO_2. In these C-V characteristics, no *bumps*, related to the presence of interface traps, are observed. Keeping in mind the care that has to be paid with respect to the interpretation of results from the conductance method with these materials, the extracted D_{it} of 1×10^{12} cm^{-2} eV^{-1} for 5 nm Al_2O_3 and 5×10^{12} cm^{-2} eV^{-1} for 5 nm HfO_2 should therefore be regarded as upper limit values.

Figure 6.29 (b) shows that for the 1.4% strained Ge MOS structure, the inversion capacitance is close to the accumulation capacitance at 300 K and 1 MHz. With the effect of strain in Ge, the weak inversion, related to minority carriers, appears before the depletion, which is related to the majority carriers. The inversion therefore occurs at smaller applied bias and becomes stronger when the bandgap energy decreases, *i.e.* when the strain in the Ge layer increases, for instance. As already demonstrated in the previous simulations, the minority carriers remain able to follow the applied bias frequency, too, up to 1 MHz.

The temperature dependence of the C-V characteristics for HfO_2 gate stacks is explored in Fig. 6.29 (c)-(f). At lower temperatures, the reduced inversion response qualitatively translates into a steeper slope in depletion. At these low temperatures, the extracted D_{it} values are restricted to a range of energies closer to the band edge, though [204]. At 80 K, D_{it} values of 4.1×10^{12} cm^{-2} eV^{-1} for HfO_2 on 1.1% strained Ge and as low as 2.9×10^{12} cm^{-2} eV^{-1} for the strained GeSn MOS structures are extracted.

Semiconductor bandgaps increase when the temperature decreases. The direct bandgap energy of Ge is about 0.8 eV. The bandgap energy of bulk Ge increases by about 0.07 eV when the temperature goes from 300 K down to 80 K. Assuming the same temperature dependence of the bandgap for strained Ge and GeSn, we note the same C-V characteristics for the 1.1% strained Ge (Fig. 6.29 (c)) and strained GeSn (Fig. 6.29 (e)) at 80 K, which are close to that of the Ge-VS at RT. Similarly, for 1.4% biaxial tensile strained Ge, the bandgap energy increases from 0.54 eV to 0.63 eV when

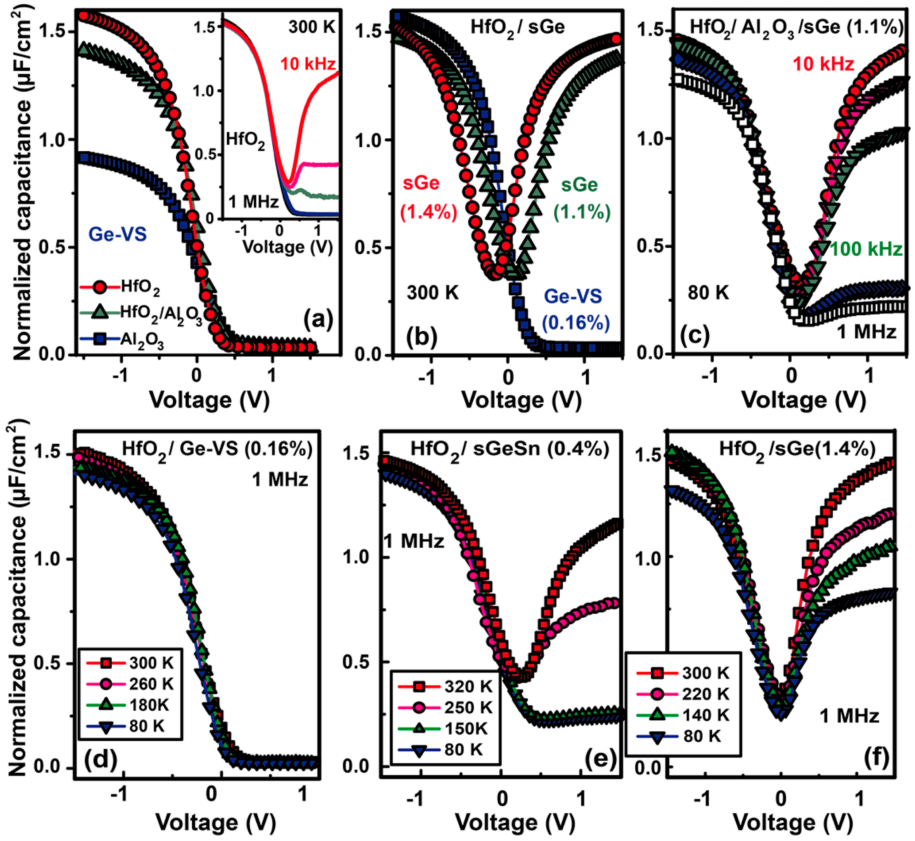


Figure 6.29: (a) C-V curves of different high-k stacks on Ge-VS measured at 1 MHz and 300 K. Frequency dispersion is shown in inset; (b) comparison of C-V at 1 MHz for 5 nm HfO_2 on Ge-VS and on 1.1% and 1.4% strained Ge, respectively. (c) Effect of frequency on the C-V response for 1 nm Al_2O_3/4 nm HfO_2/Ge (1.1% strain) structure at 80 K. (d-f) Temperature dependence of 1 MHz C-V characteristics for 5 nm HfO_2 on (d) Ge-VS, (e) strained GeSn (0.4%) and (f) strained Ge (1.4%). Figure reproduced courtesy of Wirths *et al.* [204].

the temperature drops from 300 K to 80 K. As a consequence, the inversion response should also be less pronounced, as opposed to the strong inversion response that is still present in Fig. 6.29 (f). The investigation of the effect mobility on the inversion response through the simulations allows to suggest an interpretation. Indeed, as it has been shown that the inversion response increases with the electron (minority carriers) mobility (Fig. 6.27), the difference observed in Fig. 6.29 (f) is an indication of enhanced electron mobility in Ge under tensile strain, in addition to the bandgap narrowing effect.

6.5 Equivalent circuit analysis of GeSn capped MOS structures

Direct deposition of high-k oxides, such as Al_2O_3, on GeSn is indeed associated with a high interface traps concentrations [206, 207]. A good quality IL is therefore necessary, which is usually obtained by deposition of a Ge or Si cap layer [83, 200]. It is subsequently oxidized in order to obtain the final IL. Several IL materials have been suggested, such as SiO_2, Ge, GeO_2 or $GeSnO_2$.

In this Section, we discuss the characterization of GeSn MOS structures with two different interfacial layers (IL): GeO_2 and $GeSnO_2$. As these samples show a high leakage current through the oxide, which cannot be accounted for by our numerical model, the associated simulation tool is not easily used in this situation. We will, instead, build an equivalent electrical circuit model, which is fitted to the impedance measurements performed on the samples. This method allows to deduce information on the traps that are expected to be present in the two GeO_2 and $GeSnO_2$ structures.

6.5.1 Samples

The samples consist in MOS capacitor structures based on a thin GeSn layer grown on top of a Ge virtual substrate on a Si wafer. The GeSn layer is grown at 320 °C by CVD in an ASM-Epsilon™-like reactor, using Ge_2H_6 and $SnCl_4$ precursors. The GeSn layer is 30 nm thick and the Sn concentration is 7%. The Ge virtual substrate is 1 µm thick. A thin layer of Germanium oxide is subsequently grown by Molecular Beam Epitaxy (MBE), with or without a Sn source during the growth, resulting in the fabrication of two different samples, one with a GeO_2 layer and one with a $GeSnO_2$ layers. Neither the GeSn layer or the Ge layer are intentionally doped. A 9 nm

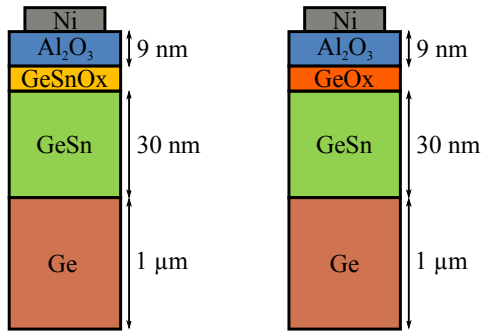


Figure 6.30: Schematic of the experimental MOS structure with GeSnOx or GeOx interfacial oxide layers.

Layer	GeO_x	$GeSnO_x$
Ge	$220 - 230$ nm	250 nm
GeSn	$38 - 44$ nm	41 nm
Al_2O_3	$14 - 14.5$ nm	$13 - 14$ nm

Table 6.2: Layer thicknesses in the sample structures, as measured by TEM.

Al_2O_3 layer is then grown on both samples, with a Ni gate to contact the structure (see Fig. 6.30).

TEM inspection reveals no visible structural defects of the GeSn and Ge layers. Only threading dislocations are present at the Ge/Si interface. The GeO_x and $GeSnO_x$ layers cannot be observed on the TEM microscopy, although their impact will be shown to strongly affect the electrical characteristics. Moreover, vacancies are visible in the oxide, which could lead to the presence of border traps. Finally, the actual thicknesses of the layers have been measured and are reported in Table 6.2. The Ge layer is actually much thinner than intended, whereas the GeSn layer is a little bit thicker than expected.

Temperature dependent DLTS measurements enable to estimate the activation energy and capture cross section of possible defects in those samples. In the sample with the GeO_2 oxide, two bulk defects are detected: one at with an activation energy $E_t - E_v = 143$ meV and another with $E_t - E_v = 291$ meV. The first one is associated with point defects and an estimated capture cross section of 6.8×10^{-16} cm^2, while the second one

Activation energy ($E_t - E_v$)	Defect type	Capture cross section
143 meV	Point defect	6.8×10^{-16} cm^2
291 meV	Threading dislocation	1.1×10^{-15} cm^2
289 meV	Interface or border trap	7.3×10^{-17} cm^2
365 meV	Interface or border trap	5.7×10^{-17} cm^2

Table 6.3: DLTS information on the traps in the two MOS samples, as determined in Ref. [29].

is related to threading dislocations and its capture cross section is around 1.1×10^{-15} cm^2. Two more traps are detected by the DLTS measurements, which are assumed to be either interface traps or border traps, *i.e.* traps located in the oxide, close the interface with the semiconductor. Possible activation energies for those two interface traps are 289 meV and 365 meV. The detection of those trap energies results from measurements on the GeO_2 sample, but DLTS measurements on the $GeSnO_2$ sample revealed similar activation energies, although their concentration is expected to be higher than in the GeO_2 sample. The much larger leakage current observed in the $GeSnO_2$ samples also tends to confirm the presence of a raised traps concentration in this sample. The results [29] are summarized in Table 6.3.

6.5.2 Impedance data and electrical model

Impedance measurements have been performed on both samples as a function of temperature, from $T = 80$ K to $T = 200$ K. Both the amplitude of the real and imaginary parts of the impedance decrease when the temperature increase. This is the case for the GeO_2 as well as the $GeSnO_2$ sample, although the variation is much larger in the case of the $GeSnO_2$. Figures 6.31 (a) and (b) show that the peaks in the reactance (X) and the plateaus in the resistance plots are also less visible at high temperature than at, e.g., $T = 80$ K.

An equivalent electrical model is then constructed. Various models have been envisioned (see Appendix D) but only the best fitting model is discussed here and schematically represented in Fig. 6.32. This model comprises the minimum number of elements to account for all expected properties of the sample, although it already involves as much as 7 elements. Those are the

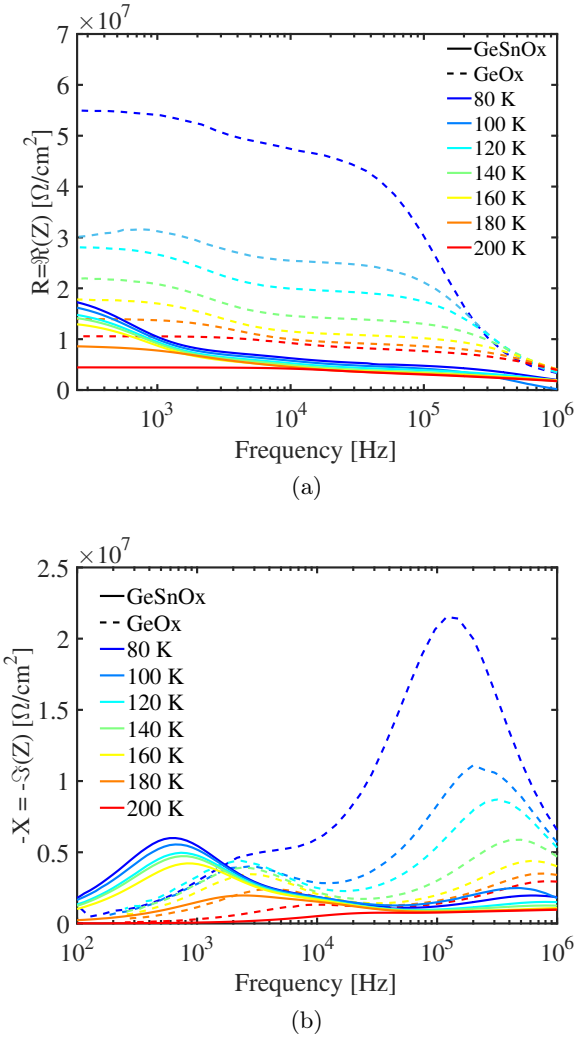


Figure 6.31: (a) Resistance R (real part of the impedance) and (b) opposite of the reactance X (imaginary part of the impedance) of both $GeSnO_2$ (full lines) and GeO_2 (dashed lines) samples as a function of frequency, for temperatures between 80 K and 200 K.

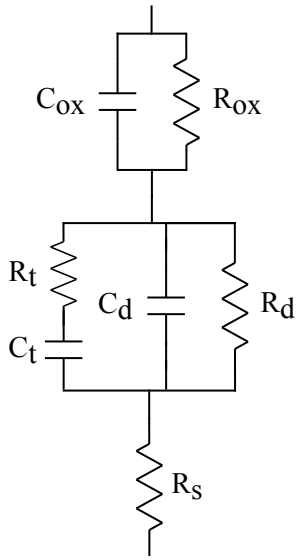


Figure 6.32: Equivalent electrical model for the GeSnOx sample.

oxide capacitance C_{ox} and a parallel resistance R_{ox} to account for leakage through the oxide. In series with these two elements is the parallel couple of the depletion capacitance C_d and accompanying resistance R_d. In order to model the presence of interface traps, an R_tC_t series couple is added in parallel to the depletion capacitance. Finally an R_s resistance is added in series with the whole model to account for the series resistance through the bulk of the semiconductor, the contacts, and the external wires.

Figures 6.31 (a) and (b) show the cut-off frequencies and peaks. The peaks that are visible in the imaginary part of the impedance are therefore related to capacitance components in the samples, in particular the depletion capacitance and the capacitance related to the presence of interface traps. The corresponding steps in the real part of the impedance are also visible and are related to the transition of the conduction pathway being directed from some branches in the equivalent model to other ones.

As the impedance features are best observed at low temperatures, this electric model is fitted to the impedance data at 90 K and the result is shown in Fig. 6.33. The values of the components obtained from the fitting are: $R_{ox} = 5.67$ kΩ, $C_{ox} = 5.31 \times 10^{-2}$ nF, $R_d = 17.1$ kΩ, $C_d = 3.48$ nF, $R_t = 5.46$ kΩ, $C_t = 8.78$ nF and $R_s = 277.7\,\Omega$. While the impedance data is only available up to 1 MHz, the modeled impedance is plotted up

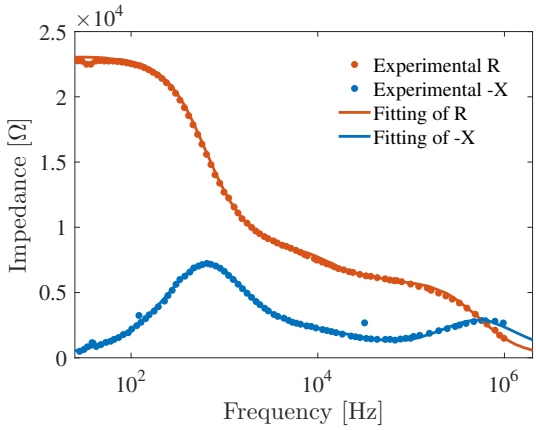


Figure 6.33: Fitting of the equivalent electrical model to the impedance data of the GeSnOx sample at 90 K and 0 V bias.

to 10 MHz to show the complete reactance peak and the resistance plateau at high frequency. From the extracted parameters, the characteristic time of the defects is $\tau_{it} = R_t C_t = 4.8 \times 10^{-5}$ s. Setting the oxide resistance R_{ox} to infinity in the equivalent model, leakage conduction through the oxide is removed and the corresponding cut-off frequency tends to zero. The decomposition of the distinctive contribution of the components in the model to the total impedance then allows to distinguish between the reactance peaks related to the depletion and the traps. This removal of R_{ox} also allows to compare the impedance spectrum with simulations involving a trap state. The similar resulting impedance curves confirm the hypothesis of the presence of a trap state with the mentioned time constant. More details on the analysis of the various electrical circuit model on these samples are provided in Appendix D.

6.6 Conclusions

In this Chapter, the consequences of materials such as GeSn, with a small bandgap as compared to Si, on the electrical properties and the application of interface traps characterization techniques in MOS structures are investigated.

C-V characteristics are first explored. Properties that can be extracted from typical C-V characteristics are demonstrated and the impact of the presence of interface traps on those characteristics is assessed. Parameters

such as the density of traps, their energy position in the bandgap, the possible presence of fixed charges in the oxide and the effect of temperature are investigated. Charges in the oxide are shown to shift the V_{fb} value, in particular.

As a subsequent step, the conductance method is examined as it is applied to GeSn materials. Interface traps with discrete energy levels and extended energy distributions are reviewed, highlighting one of the main issues of the method, which is the confusion of the inversion response with the expected conductance response related to the D_{it} value. This is shown to lead to inaccurate extraction of the D_{it} value and even, in some case, to totally impair the detection of interface traps. The variation of the interface Fermi level with the applied bias depends strongly on the presence on interface traps and their concentration. The key parameters affecting the interface traps time constant are then discussed, as well as their ability to estimate the interface energy position.

The specific conditions leading to an enhanced or reduced inversion response are then explored. The impact of a reduced bandgap energy is shown to increase the inversion response. The effect of the charge carriers mobilities and effective masses is also noted. This information is subsequently used to contribute to the interpretation of experimental C-V characteristics from strained Ge and strained GeSn layers. They allow to distinguish the origin of an enhanced inversion response and reveal the presence of higher mobility carriers in strained Ge (1.4%) layers by attributing a strong inversion response at 80 K to this enhanced carrier mobility.

Finally, experimental MOS structures with two different oxide interlayers are presented and impedance measurements are performed on them. Fitting of an electrical model to this data results in the obtention of electrical parameters related to the physical elements of the sample and the detection of the presence of a trap level. A characteristic time for the interface traps is determined from those values.

Chapter 7

Conclusions

In this work, the impact of electron trap states in GeSn materials has been assessed by electrical characterization methods. Alloying Sn with Ge in GeSn semiconducting heterostructures naturally leads to a relatively large concentration of structural defects. These can act as electron trap states and, in combination with the low bandgap of GeSn materials, their influence is both substantial and potentially difficult to evaluate.

Two main types of semiconducting structures were investigated: p-GeSn/ n-Ge junctions and GeSn based MOS structures. Our goal was to analyze those systems using a wide range of electrical techniques to deeply understand the impact of electron trap states on the transport properties of GeSn based materials. Current-voltage characteristics, capacitance-voltage characteristics, admittance spectroscopy and time-dependent measurements of the electric current were harnessed to extract information from the experimental devices. Numerical simulations allowed to provide interpretations to those results. Those simulations also made possible the exploration of the comportment of these structures under a variety of conditions, in order to highlight the key parameters and their impact on the characterization of electron trap states in GeSn materials. An additional approach to the interpretation of experimental results was provided by equivalent electrical circuits modeling. This technique is best applied to situations where the numerical simulations cannot be properly performed because of the limiting modeling hypotheses. The representation of the devices by lumped elements allowed to reproduce the experimental data to a certain extent. The role of each element provided helpful information on the microscopic processes which could induce those transport properties, by analyzing how the variation of distinct element values affects the resulting characteristics.

A model based on the resolution of the basic semiconductor equations, *i.e.* Poisson's equation and the charge carriers continuity equations explicitly including a rate equation for the trap levels, was developed in Chapter 4. This method provided a systematic way to evaluate the impact of most physical properties of trap states, such as their energy position in the bandgap, their concentration and capture cross section. All microscopic parameters set as inputs to the numerical simulations can, in theory, be extracted from the output characteristics, depending on the magnitude of their influence on those curves. In practical situations, though, only a reduced set of those parameters is generally relevant to the interpretation of experimental data. The specific impact of the various remaining quantities on the output characteristics as a function of frequency, applied bias or temperature further allowed to separate them from each other. Iteratively adapting those relevant parameters values to fit the experimental data enabled the extraction of the corresponding physical parameter values.

Although numerical simulations through a dedicated software had already previously been put into use for the characterization of other types of semiconducting materials, such as III-V compounds, its operation applied to small bandgap materials involved a code refactoring. The numerical iterative procedure to solve the set of equations obtained as a result of the discretization of the fundamental equations had to be modified in order to enable proper convergence rates in the case of the specific materials. A different numerical library, in particular, had to be used to perform the inversion of the Jacobian matrix. The convergence rates were tuned, especially in the case of bias-dependent characteristics simulations. A better guess, based on the previous bias step converged result, notably had to be used.

7.1 Achievements

7.1.1 GeSn/Ge pn diodes

In the first part of the results, reported in Chapter 5, Boron doped p-GeSn/n-Ge pn junctions grown by CVD have been investigated, with a Sn content in the GeSn layer of 5.8%. The I-V characteristics revealed that the diodes were of good quality, with a reasonable ratio between the currents at +1 V and −1 V. Little effect of the presence of traps in the structure is initially indicated. The ideality factor at room temperature of 1.2 implies the occurrence of limited recombinations, though. Temperature-dependent measurements have subsequently been performed in order to evaluate the activation energy

of the reverse saturation current I_s. An activation energy of 300 meV was extracted.

Through the simulations of similar structures, this activation energy was demonstrated to result from the presence of recombination centers in the space charge region of the diode. A trap level with an energy located between 200 meV and 250 meV above the valence band is shown to be best able to reproduce the experimental values. This trap energy level is close to the expected energy of Sn-vacancies deep levels. An indicative concentration value of 2×10^{17} cm^{-3} was also estimated for the concentration of this trap level.

A strong bias-dependence of the total reverse current was observed. These currents larger than the extracted I_s values denote the presence of an additional, field-enhanced, transport mechanism. Based on the small bandgap energy and the recognized presence of traps, trap-assisted tunneling or band-to-band tunneling are two possible cases.

C-V measurements performed on the diodes enabled to extract the Ge substrate carrier concentration. Little frequency dispersion and overall impact of the presence of traps was observed, which is consistent with their limited spatial extension, close to the GeSn/Ge interface. A link between the maximum capacitance at small forward bias and the dopant concentration in the GeSn layer was also highlighted from the simulations, but required more experimental substantiation to be fully assessed.

The electrical response of unpassivated GeSn/Ge mesa diodes was subsequently investigated. A strong hysteretic behaviour was observed under the application of a reverse bias. Large transients were also present when the diodes are set to a fixed reverse bias and the current is measured over time. These are shown to be the consequence of the presence of native oxide on the unpassivated sidewalls. Indeed, temporarily removing this oxide by dipping the diodes in H_2O_2 eliminates all appearance of the transients and hysteresis.

The behaviour of the transients on the unpassivated diodes was then explored, in view of establishing whether information pertaining to the current actually flowing through the diode can be recovered. The transients were shifted to both larger or lower currents depending on the conditions previously applied to the diodes, though. A steady, repeatable response subsequently could not be obtained from those unpassivated diodes. Temperature was shown to impact the amplitude of the transients, and the dependence of the amplitude with the applied bias is also noted. An activation energy for

the final current after a determined transient duration was also extracted from the temperature measurements, which also showed a maximum activation energy for a bias value of −1 V. A bias dependent competition mechanism between the charging of the traps in the native oxide on the sidewalls and the current actually flowing through the diode was therefore suggested.

Modeling of the transient response with an equivalent electrical model circuit was eventually proposed. A combination of several RC couples with different time constants was advanced, in order to accurately account for the shape of the transients. The initial fast growing current, on the other hand, was modeled by an inductive element. This inductive behaviour is linked with a large transit time of electrons through the native oxide. Extrapolation of the modeled transient current until it reaches a value equal to that of the H_2O_2 passivated diode indicates that filling all the traps in the native oxide on the sidewalls might take as long as two weeks. Only then would the transient response be removed and a steady current reached.

7.1.2 GeSn MOS devices

In the second part of the results, reported in Chapter 6, we evaluated the impact of electron traps in MOS structures made out of small bandgap materials, such as GeSn, on their electrical properties and the methods usually employed for their characterization.

We first explored C-V characteristics of GeSn MOS structures in the presence of interface traps. The extraction of traps properties from typical features such as the *bumps* in those C-V curves was demonstrated. Their dependence on the interface traps energy and density was thoroughly evaluated. The influence of the presence of fixed charges in the oxide, although not altering the C-V *bump*, was shown to shift the value of V_{fb} by an amount that depends on the distance between those traps and the oxide gate. The deviation of V_{fb} is therefore even more important when the oxide thickness is modified.

The application of the conductance method to GeSn MOS structures was then examined. Discrete energy interface traps were first simulated and the effect of their energy position and density were analyzed. The interface trap density was shown to be accessible through the conductance method, with the exception of traps located at an energy position where the inversion response starts to dominate their conductance signal. We demonstrated that the value of D_{it} could potentially be overestimated and the presence of interface traps could even be totally concealed by this inversion response.

Traps with more extended energy distributions were also considered and a relationship between their D_{it} and the conductance signal was demonstrated.

The energy position of the traps, though, could not directly be assessed by the value of the applied bias. The Fermi level displacement with the applied bias was indeed revealed as strongly dependent on the interface traps energy and density, thus preventing the estimation of the position of the interface Fermi level for a given applied bias. To determine the energy of the detected traps, the use of the peak frequency corresponding to the interface traps time constant was discussed. The peak frequency enabled to successfully determine the traps energy, provided that some parameters such as the interface traps capture cross section are known or accurately estimated. The accessibility of an interface trap energy because of its corresponding interface trap constant and the related measurement frequency that is required was also shown.

We subsequently studied the conditions affecting the onset of the inversion response. The reduction of the bandgap energy was found to dramatically enhance the inversion response. The mobility of minority carriers also strongly impacted the inversion response, while the mobility of majority carriers had no such effect. The effective masses also alter slightly the strength of the inversion response, but to a much lower extent. The knowledge gained from those simulations was then bestowed to the interpretation of experimental C-V characteristics from strained Ge and strained GeSn layers. They allowed to explain the origin of the high inversion response found in lower bandgap materials. The determination of the inversion response dependence on minority carrier mobility also supported the attribution of a strong inversion observed in strained Ge (1.4%) layers at 80 K to the presence of an enhanced carrier mobility in this sample.

Finally, experimental MOS structures with two oxide interfacial layers were presented: one with a GeO_2 and another with a $GeSnO_2$ interlayer. The strong leakage current of these samples prevented the application of the numerical modeling software and an equivalent electrical circuit modeling was performed instead. A model including the presence of a trap state was shown to best fit to the impedance data, thereby confirming the presence of such a trap. An increased concentration of traps in the sample with the $GeSnO_2$ interlayer as compared to the GeO_2 interlayer was also observed.

7.2 Perspectives

Numerous additional investigations could have been performed to further support and expand the conclusions reached in this work. Some of them were plainly out of the scope of this work, others could not be completed because of practical difficulties related to the experimental setups and availability of suitable samples, or insufficient refinement of the numerical model and, of course, because of limited time.

In particular, the numerical model could be expanded to take into account TAT or BTBT. This would provide more insight into the behaviour of small bandgap materials such as GeSn. The development of a two-dimensional version of the numerical simulation code has also been initiated during the course of this research, as it would provide a significant improvement to the range of devices that could be simulated. Three-contact devices such as full MOSFET transistors could thereby be modeled. This new simulation code could not progress beyond the resolution of the steady-state equations, though, because of huge difficulties encountered in obtaining a resolution process that could converge reliably. Further development of this code has therefore been halted, so as not to impair the pursuance of other facets of this work. Completion of this new simulation software, however, will open up many improved possibilities regarding the simulations of GeSn based devices.

In the course of this work, the research field related to GeSn materials has evolved tremendously, but also sometimes changed direction. Although the focus initially was on transistor devices with improved mobility performance, the spotlight subsequently turned to optical applications. This shift was partly related to the recurring difficulties involved in experimental research to obtain sufficiently defect-free GeSn layers and the breakthrough associated with the obtention of direct bandgap materials, be it direct bandgap GeSn or direct bandgap Ge through the strain induced by GeSn or even SiGeSn materials.

In this regard, an opto-electrical setup was developed as part of this work. The setup is intended to provide useful capabilities both for the characterization of electrically active defects and the general optical characterization of GeSn layers. It consists in a spectrometer and an IR light source coupled with an IR light detector and a fast electrical current acquisition apparatus. The goal is to investigate the electrical current collected on a test device under illumination with a light of variable energy. The properties of traps located anywhere in the bandgap can thus be probed, this time dealing with

optical capture cross sections instead of the thermal capture cross sections involved in plain electrical measurements. The setup, although completed and apt to provide absorption measurements, has not yet been able to be put into practical use regarding the simultaneous detection of a photocurrent related to a given incident light energy, mainly because of non-optimized sample structures. Once completed, it could provide very interesting complementary information on the defects in GeSn materials.

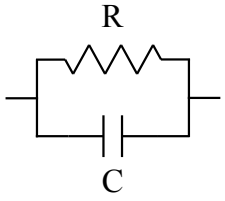
It is our ambition that this work has provided new and interesting information on the impact of electronic trap states in GeSn semiconducting structure. Our numerical simulation tool proved to be a powerful technique to leverage crucial information on the traps present in GeSn/Ge diodes. We also hope and expect that our findings will be valuable to other researchers to better understand the influence of critical physical parameters of interface traps and the way that their accurate characterization can be enabled or prevented.

Appendix A

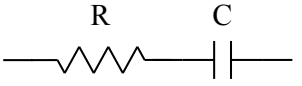
Equivalent electrical model

In this appendix, the analytical expressions for the impedance, admittance and their real and imaginary parts are developed for various equivalent electrical model circuits.

A.1 Parallel RC and RC series circuits

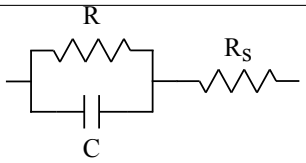


τ	
Z	$\dfrac{R}{1+j\omega\tau}$
$\Re[Z]$	$\dfrac{R}{1+\omega^2\tau^2}$
$-\Im[Z]$	$\dfrac{R\omega\tau}{1+\omega^2\tau^2}$
Y	$\dfrac{1+j\omega\tau}{R}$
$\Re[Y]$	$\dfrac{1}{R}$
$\Im[Y]$	ωC



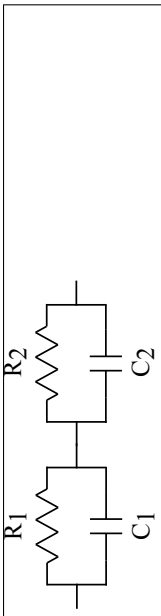
RC	
Z	$R+\dfrac{1}{j\omega C}$
$\Re[Z]$	R
$-\Im[Z]$	$\dfrac{1}{\omega C}$
Y	$\dfrac{j\omega C}{1+j\omega\tau}$
$\Re[Y]$	$\dfrac{\omega^2\tau C}{1+\omega^2\tau^2}$
$\Im[Y]$	$\dfrac{\omega C}{1+\omega^2\tau^2}$

A.2 Parallel RC circuit with a series resistance

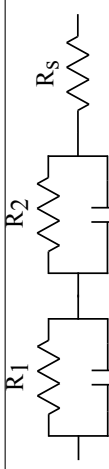


τ	RC
Z	$\frac{R}{1+j\omega\tau} + R_s$
$\Re[Z]$	$\frac{R}{1+\omega^2\tau^2} + R_s$
$-\Im[Z]$	$\frac{R\omega\tau}{1+\omega^2\tau^2}$
Y	$\frac{1+j\omega\tau}{R+R_s+j\omega\tau R_s}$
$\Re[Y]$	$\frac{R+R_s+R_s\tau^2\omega^2}{(R+R_s)^2+\omega^2\tau^2R_s^2}$
$\Im[Y]$	$\frac{\omega R\tau}{(R+R_s)^2+\omega^2\tau^2R_s^2}$

A.3 Two parallel RC circuits in series

	
τ_1	R_1C_1
τ_2	R_2C_2
Z	$\frac{R_1}{1+j\omega\tau_1}+\frac{R_2}{1+j\omega\tau_2}$
$\Re[Z]$	$\frac{R_1}{1+\omega^2\tau_1^2}+\frac{R_2}{1+\omega^2\tau_2^2}$
$-\Im[Z]$	$\frac{R_1\omega\tau_1}{1+\omega^2\tau_1^2}+\frac{R_2\omega\tau_2}{1+\omega^2\tau_2^2}$
Y	$\frac{j\left(-j+\omega\tau_1\right)\left(-j+\omega\tau_2\right)}{R_1\left(-j+\omega\tau_2\right)+R_2+j\omega\left(R_2\tau_1+R_1\tau_2\right)}$
$\Re[Y]$	$\frac{R_1+R_2+R_1\omega^2\tau_2^2+R_2\omega^2\tau_1^2}{R_1^2\left(1+\omega^2\tau_2^2\right)+R_2^2\left(1+\omega^2\tau_1^2\right)+2R_1\left(R_2+R_2\omega^2\tau_1\tau_2\right)}$
$\Im[Y]$	$\frac{\omega R_1\tau_1+\omega R_2\tau_2+\omega^2R_1\tau_1\tau_2^2+\omega^2R_2\tau_2\tau_1^2}{\left(R_1+R_2\right)^2+\omega^2\left(R_2\tau_1+R_1\tau_2\right)^2}$

A.4 Two parallel RC circuits and a series resistance

	
τ_1	R_1C_1
τ_2	R_2C_2
Z	$\frac{R_1}{1+j\omega\tau_1}+\frac{R_2}{1+j\omega\tau_2}+R_s$
$\Re[Z]$	$\frac{R_1}{1+\omega^2\tau_1^2}+\frac{R_2}{1+\omega^2\tau_2^2}+R_s$
$-\Im[Z]$	$\frac{R_1\omega\tau_1}{1+\omega^2\tau_1^2}+\frac{R_2\omega\tau_2}{1+\omega^2\tau_2^2}$
Y	$\frac{(1+j\omega\tau_1)(1+j\omega\tau_2)}{R_1(1+j\omega\tau_2)+R_2(1+j\omega\tau_1)+R_S(1+j\omega\tau_1+j\omega\tau_2-\omega^2\tau_1\tau_2)}$
$\Re[Y]$	$\frac{R_1\left(1+\omega^2\tau_2^2\right)+R_2\left(1+\omega^2\tau_1^2\right)+R_s\left(1+\omega^2\left(\tau_2^2+\tau_1^2+\omega^2\tau_1^2\tau_2^2\right)\right)}{\left(R_1+R_2+R_s\right)^2+\left(R_1+R_s\right)^2\omega^2\tau_2^2+\left(R_2+R_s\right)^2\omega^2\tau_1^2+2R_1R_2\omega^2\tau_1\tau_2+R_s^2\omega^4\tau_1^2\tau_2^2}$
$\Im[Y]$	$\frac{R_1\omega\tau_1+R_2\omega\tau_2+\omega^3\tau_1\tau_2\left(R_1\tau_2+R_2\tau_1\right)}{\left(R_1+R_2+R_s\right)^2+\left(R_1+R_s\right)^2\omega^2\tau_2^2+\left(R_2+R_s\right)^2\omega^2\tau_1^2+2R_1R_2\omega^2\tau_1\tau_2+R_s^2\omega^4\tau_1^2\tau_2^2}$

Appendix B

Linearization of the discretized equations

The procedure of linearization of the discretized semiconductor equations developed in Chapter 4 is exposed in this appendix. The linearized coefficients of Poisson's equation (Eq. (4.64)) and electrons (Eq. (4.77)), holes (Eq. (4.78)) and trapped level (Eq. (4.79)) continuity equations are used in the Newton method iterations to the solution.

Differentiation is performed using the relations (4.92), (4.93) and (4.94) in the discrete semiconductor equations.

B.1 Poisson's equation

Starting from Eq. (4.64):

$$\lambda_0^2 \left[a_{i-1}\psi_{i-1} + a_i\psi_i + a_{i+1}\psi_{i+1}\right] - n_i + N_D^+ + p_i - N_A^- + n_{t,i}^* = 0 \quad \text{(B.1)}$$

Differentiation of all the terms leads to

$$\begin{aligned}\lambda_0^2 a_{i-1}\delta\psi_{i-1} + \lambda_0^2 a_i\delta\psi_i + \lambda_0^2 a_{i+1}\delta_{i+1} \\ - n_i\left(\delta F_{n,i} + \delta\psi_i\right) - p_i\left(\delta\psi_i + \delta F_{p,i}\right) - n_{t,i}\beta_i\left(\delta\psi_i + \delta F_{t,i}\right)\end{aligned} \quad \text{(B.2)}$$

and rearranging the terms for each variables, the linearized Poisson's equation is obtained:

$$\left[\lambda_0^2 a_{i-1}\right]\delta\psi_{i-1} + \left[\lambda_0^2 a_i - n_i - p_i - n_{t,i}\beta_i\right]\delta\psi_i + \left[\lambda_0^2 a_{i+1}\right]\delta\psi_{i+1} + \left[-n_i\right]\delta F_{n,i} + \left[-p_i\right]\delta F_{p,i} + \left[-n_{t,i}\beta_i\right]\delta F_{t,i} = 0 \quad \text{(B.3)}$$

B.2 Electron continuity equation

From the discrete electron continuity equation (4.77)

$$\begin{aligned} &\frac{2\mu_n^{i+1/2}}{h_i\left(h_i + h_{i-1}\right)}\left[B\left(\psi_{i+1} - \psi_i\right)n_{i+1} - B\left(\psi_i - \psi_{i+1}\right)n_i\right] \\ -&\frac{2\mu_n^{i-1/2}}{h_{i-1}\left(h_i + h_{i-1}\right)}\left[B\left(\psi_i - \psi_{i-1}\right)n_i - B\left(\psi_{i-1} - \psi_i\right)n_{i-1}\right] \\ &-R_{n,i} \qquad\qquad = \quad 0 \end{aligned} \quad \text{(B.4)}$$

we define the following quantities, among which are particular values of the Bernoulli function B, in order to shorten the next expressions,

$$\begin{aligned} \mathsf{M}_n^{i+1/2} &= \frac{2\mu_n^{i+1/2}}{h_i\left(h_i + h_{i-1}\right)} \\ \mathsf{M}_n^{i-1/2} &= \frac{2\mu_n^{i-1/2}}{h_{i-1}\left(h_i + h_{i-1}\right)} \end{aligned}$$

$$\begin{aligned} \mathsf{B}_-^{i+1/2} &= B\left(\psi_{i+1} - \psi_i\right) & \mathsf{B}_-^{i-1/2} &= B\left(\psi_i - \psi_{i-1}\right) \\ \mathsf{B}_+^{i+1/2} &= B\left(\psi_i - \psi_{i+1}\right) & \mathsf{B}_+^{i-1/2} &= B\left(\psi_{i-1} - \psi_i\right) \end{aligned}$$

$$\begin{aligned} \mathsf{B}'^{i+1/2}_- &= \frac{\mathrm{d}B\left(\psi_{i+1} - \psi_i\right)}{\mathrm{d}\left(\psi_i - \psi_{i+1}\right)} & \mathsf{B}'^{i-1/2}_- &= \frac{\mathrm{d}B\left(\psi_i - \psi_{i-1}\right)}{\mathrm{d}\left(\psi_{i-1} - \psi_i\right)} \\ \mathsf{B}'^{i+1/2}_+ &= \frac{\mathrm{d}B\left(\psi_i - \psi_{i+1}\right)}{\mathrm{d}\left(\psi_i - \psi_{i+1}\right)} & \mathsf{B}'^{i-1/2}_+ &= \frac{\mathrm{d}B\left(\psi_{i-1} - \psi_i\right)}{\mathrm{d}\left(\psi_{i-1} - \psi_i\right)} \end{aligned}$$

which allows to rewrite Eq. B.4 as

$$\mathsf{M}_n^{i+1/2}\left[\mathsf{B}_-^{i+1/2}n_{i+1} - \mathsf{B}_+^{i+1/2}n_i\right] - \mathsf{M}_n^{i-1/2}\left[\mathsf{B}_-^{i-1/2}n_i - \mathsf{B}_+^{i-1/2}n_{i-1}\right] - R_{n,i} = 0 \quad \text{(B.5)}$$

Differentiation all the terms yields

$$\mathsf{M}_n^{i+1/2}\left[\mathsf{B}_-^{i+1/2}\delta n_{i+1}-\mathsf{B}_+^{i+1/2}\delta n_i+\mathsf{B}'^{i+1/2}_-\delta\left(\psi_{i+1}-\psi_i\right)n_{i+1}-\mathsf{B}'^{i+1/2}_+\delta\left(\psi_i-\psi_{i+1}\right)n_i\right]$$

$$-\mathsf{M}_n^{i-1/2}\left[\mathsf{B}_-^{i-1/2}\delta n_i-\mathsf{B}_+^{i-1/2}\delta n_{i-1}+\mathsf{B}'^{i-1/2}_-\delta\left(\psi_i-\psi_{i-1}\right)n_i-\mathsf{B}'^{i-1/2}_+\delta\left(\psi_{i-1}-\psi_i\right)n_{i-1}\right]-\delta R_{n,} \tag{B.6}$$

The recombination term $\delta R_{n,i}$ is decomposed, using Eq. (4.22) and (4.21), into its constituents

$$\delta R_{n,i}=\delta r_{n,i}+\delta r_{bb,i}$$

which are further differentiated as

$$\begin{aligned}\delta r_{n,i} &= c_n\left(N_t-n_{t,i}\right)\delta n_i-c_n\,n_i\,\delta n_{t,i}-c_n\,g_t\,n_\bigstar\,\delta n_{t,i}\\ &= c_n\left[n_i\left(N_t-n_{t,i}\right)-n_i n_{t,i}\beta_i-g_t n_\bigstar n_{t,i}\beta_i\right]\delta\psi_i\\ &\quad +c_n\left[n_i\left(N_t-n_{t,i}\right)\right]\delta F_{n,i}\\ &\quad +c_n\left[-\left(n_i+g_t n_\bigstar\right)n_{t,i}\beta_i\right]\delta F_{t,i}\end{aligned} \tag{B.7}$$

$$\begin{aligned}\delta r_{bb,i} &= B_r\left(n_i\delta p_i+p_i\delta n_i\right)\\ &= B_r\left(-n_i p_i\delta\left(\psi_i+F_{p,i}\right)+p_i n_i\delta\left(\psi_i+F_{n,i}\right)\right)\\ &= \left[B_r n_i p_i\right]\delta F_{n,i}-\left[B_r n_i p_i\right]\delta F_{p,i}\end{aligned} \tag{B.8}$$

with

$$n_\bigstar=N_c e^{\dfrac{E_t-E_c}{kT}} \tag{B.9}$$

Inserting all these into Eq. (B.6) and reordering the terms as a function of each variable, the following coefficients are obtained:

$$
\begin{aligned}
&\left[-\mathsf{M}_n^{i-1/2}\left(-\mathsf{B}_+^{i-1/2}n_{i-1}-\mathsf{B}'^{i-1/2}_{-}n_i-\mathsf{B}'^{i-1/2}_{+}n_{i-1}\right)\right] && \delta\psi_{i-1}\\
&+\left[-\mathsf{M}_n^{i-1/2}\left(-\mathsf{B}_+^{i-1/2}n_{i-1}\right)\right] && \delta F_{n,i-1}\\
&+0 && \delta F_{p,i-1}\\
&+0 && \delta F_{t,i-1}\\
&+\Bigg[\mathsf{M}_n^{i+1/2}\left[-\mathsf{B}_+^{i+1/2}n_i+\left(\mathsf{B}'^{i+1/2}_{-}n_{i+1}-\mathsf{B}'^{i+1/2}_{+}n_i\right)\right]\\
&\quad-\mathsf{M}_n^{i-1/2}\left[\mathsf{B}_-^{i-1/2}n_i-\left(\mathsf{B}'^{i-1/2}_{-}n_i-\mathsf{B}'^{i-1/2}_{+}n_{i-1}\right)\right]\\
&\quad-c_n\left[n_i\left(N_t-n_{t,i}\right)-n_i\,n_{t,i}\,\beta_i-g_t\,n_\bigstar\,n_{t,i}\beta_i\right]\Bigg] && \delta\psi_i\\
&+\left[-\mathsf{M}_n^{i+1/2}\mathsf{B}_+^{i+1/2}n_i-\mathsf{M}_n^{i-1/2}\mathsf{B}_-^{i-1/2}n_i-c_n\,\left[n_i\left(N_t-n_{t,i}\right)\right]-B_r\,n_i\,p_i\right] && \delta F_{n,i}\\
&+\left[B_r\,n_i\,p_i\right] && \delta F_{p,i}\\
&+\left[c_n\,\left(n_i+g_tn_\bigstar\right)n_{t,i}\beta_i\right] && \delta F_{t,i}\\
&+\left[\mathsf{M}_n^{i+1/2}\left[\mathsf{B}_-^{i+1/2}n_{i+1}-\left(\mathsf{B}'^{i+1/2}_{-}n_{i+1}-\mathsf{B}'^{i+1/2}_{+}n_i\right)\right]\right] && \delta\psi_{i+1}\\
&+\left[\mathsf{M}_n^{i+1/2}\left(\mathsf{B}_-^{i+1/2}n_{i+1}\right)\right] && \delta F_{n,i+1}\\
&+0 && \delta F_{p,i+1}\\
&+0 && \delta F_{t,i+1} \quad = 0
\end{aligned}
$$

B.3 Hole continuity equation

From the discrete hole continuity equation (4.78)

$$
\begin{aligned}
&\frac{2\mu_p^{i+1/2}}{h_i\left(h_i+h_{i-1}\right)}\left[B\left(\psi_{i+1}-\psi_i\right)p_i-B\left(\psi_i-\psi_{i+1}\right)p_{i+1}\right]\\
&-\frac{2\mu_p^{i-1/2}}{h_{i-1}\left(h_i+h_{i-1}\right)}\left[B\left(\psi_i-\psi_{i-1}\right)p_{i-1}-B\left(\psi_{i-1}-\psi_i\right)p_i\right]\\
&\qquad+R_{p,i} \qquad = \quad 0
\end{aligned}
\tag{B.10}
$$

we define the following quantities

$$\begin{aligned} \mathsf{M}_p^{i+1/2} &= \frac{2\mu_p^{i+1/2}}{h_i\,(h_i+h_{i-1})} \\ \mathsf{M}_p^{i-1/2} &= \frac{2\mu_p^{i-1/2}}{h_{i-1}\,(h_i+h_{i-1})} \end{aligned}$$

which allows to rewrite Eq. B.10 as

$$\mathsf{M}_p^{i+1/2}\left[\mathsf{B}_-^{i+1/2}p_i - \mathsf{B}_+^{i+1/2}p_{i+1}\right] - \mathsf{M}_p^{i-1/2}\left[\mathsf{B}_-^{i-1/2}p_{i-1} - \mathsf{B}_+^{i-1/2}p_i\right] + R_{p,i} = 0 \tag{B.11}$$

Differentiation all the terms yields

$$\mathsf{M}_p^{i+1/2}\left[\mathsf{B}_-^{i+1/2}\delta p_i - \mathsf{B}_+^{i+1/2}\delta p_{i+1} + \mathsf{B}'^{i+1/2}_-\delta\left(\psi_{i+1}-\psi_i\right)p_i - \mathsf{B}'^{i+1/2}_+\delta\left(\psi_i-\psi_{i+1}\right)p_{i+1}\right]$$

$$-\mathsf{M}_p^{i-1/2}\left[\mathsf{B}_-^{i-1/2}\delta p_{i-1} - \mathsf{B}_+^{i-1/2}\delta p_i + \mathsf{B}'^{i-1/2}_-\delta\left(\psi_i-\psi_{i-1}\right)p_{i-1} - \mathsf{B}'^{i-1/2}_+\delta\left(\psi_{i-1}-\psi_i\right)p_i\right] + \delta R_{p,i} \tag{B.12}$$

The recombination term $\delta R_{p,i}$ is decomposed, using Eq. (4.23) and (4.21), into its constituents

$$\delta R_{p,i} = \delta r_{p,i} + \delta r_{bb,i}$$

which are further differentiated as

$$\begin{aligned} \delta r_{p,i} &= c_p\, n_{t,i}\delta p_i - c_p\, p_i\, \delta n_{t,i} - c_p\, \frac{1}{g_t}\, p_\bigstar\, \delta n_{t,i} \\ &= c_p\left[-n_{t,i}p_i - p_i\, n_{t,i}\,\beta_i - \frac{1}{g_t}p_\bigstar n_{t,i}\beta_i\right]\delta\psi_i \\ &\quad + c_p\left[-n_{t,i}\,p_i\right]\delta F_{p,i} \\ &\quad + c_p\left[\left(p_i + \frac{1}{g_t}n_\bigstar\right)n_{t,i}\beta_i\right]\delta F_{t,i} \end{aligned} \tag{B.13}$$

$$\begin{aligned} \delta r_{bb,i} &= B_r\,\left(n_i\,\delta p_i + p_i\,\delta n_i\right) \\ &= B_r\,\left(-n_i p_i \delta\left(\psi_i + F_{p,i}\right) + p_i n_i \delta\left(\psi_i + F_{n,i}\right)\right) \\ &= \left[B_r n_i p_i\right]\delta F_{n,i} - \left[B_r n_i p_i\right]\delta F_{p,i} \end{aligned} \tag{B.14}$$

with

$$p_{\bigstar} = N_v e^{\frac{E_v - E_t}{kT}} \tag{B.15}$$

Inserting all these into Eq. (B.12) and reordering the terms as a function of each variable, the following coefficients are obtained:

$$\begin{aligned}
&\left[-\mathsf{M}_p^{i-1/2}\left(-\mathsf{B}_-^{i-1/2}p_{i-1} - \mathsf{B}'^{i-1/2}_- p_{i-1} - \mathsf{B}'^{i-1/2}_+ p_i\right)\right] && \delta\psi_{i-1}\\
&\qquad +0 && \delta F_{n,i-1}\\
&\qquad + \left[-\mathsf{M}_p^{i-1/2}\left(-\mathsf{B}_-^{i-1/2}p_{i-1}\right)\right] && \delta F_{p,i-1}\\
&\qquad +0 && \delta F_{t,i-1}\\
&+\Bigg[\mathsf{M}_p^{i+1/2}\left[-\mathsf{B}_+^{i+1/2}n_i + \left(\mathsf{B}'^{i+1/2}_- p_i - \mathsf{B}'^{i+1/2}_+ p_{i+1}\right)\right]\\
&\quad -\mathsf{M}_p^{i-1/2}\left[\mathsf{B}_-^{i-1/2}p_i - \left(\mathsf{B}'^{i-1/2}_- p_{i-1} - \mathsf{B}'^{i-1/2}_+ p_i\right)\right]\\
&\quad -c_p\left[-n_{t,i}\,p_i - p_i\,n_{t,i}\,\beta_i - \frac{1}{g_t}\,p_{\bigstar}\,n_{t,i}\beta_i\right]\Bigg] && \delta\psi_i\\
&\qquad +\left[B_r\,n_i\,p_i\right] && \delta F_{n,i}\\
&+\left[-\mathsf{M}_p^{i+1/2}\mathsf{B}_-^{i+1/2}p_i - \mathsf{M}_p^{i-1/2}\mathsf{B}_+^{i-1/2}p_i + c_p\,[n_{t,i}\,p_i] - B_r\,n_i\,p_i\right] && \delta F_{p,i}\\
&\qquad +\left[c_p\left(p_i + \frac{1}{g_t}p_{\bigstar}\right)n_{t,i}\beta_i\right] && \delta F_{t,i}\\
&+\left[\mathsf{M}_p^{i+1/2}\left[\mathsf{B}_+^{i+1/2}p_{i+1} - \left(\mathsf{B}'^{i+1/2}_- p_i - \mathsf{B}'^{i+1/2}_+ p_{i+1}\right)\right]\right] && \delta\psi_{i+1}\\
&\qquad +0 && \delta F_{n,i+1}\\
&\qquad +\left[\mathsf{M}_p^{i+1/2}\left(\mathsf{B}_+^{i+1/2}p_{i+1}\right)\right] && \delta F_{p,i+1}\\
&\qquad +0 && \delta F_{t,i+1} \quad = 0
\end{aligned}$$

B.4 Trap level occupancy continuity equation

The discrete continuity equation for the occupancy of the trap level (4.79) is

$$r_{n,i} - r_{p,i} = 0 \tag{B.16}$$

Differentiating the two terms leads to

$$\delta r_{n,i} - \delta r_{p,i} = 0 \tag{B.17}$$

and expanding them into their constituents yields the linearized form of the discrete continuity equation of the traps:

$$\begin{aligned}
&\left[c_n \left[n_i\, N_t - n_i\, n_{t,i}\,(1+\beta_i) - g_t n_\bigstar n_{t,i}\beta_i\right] - c_p \left[p_i\, n_{t,i}\,(\beta_i - 1) + \frac{1}{g_t} p_\bigstar n_{t,i}\beta_i\right]\right] && \delta\psi_i \\
&\qquad + \left[c_n\, n_i\, \left(N_t - n_{t,i}\right)\right] && \delta F_{n,i} \\
&\qquad + \left[c_p\, p_i\, n_{t,i}\right] && \delta F_{p,i} \\
&+ \left[c_n \left[-\left(n_i + g_t n_\bigstar\right) n_{t,i}\beta_i\right] - c_p \left[\left(p_i + \frac{1}{g_t} p_\bigstar\right) n_{t,i}\beta_i\right]\right] && \delta F_{t,i} \quad = 0
\end{aligned}$$

Appendix C

Optoelectrical characterization of pGeSn/n$^+$Ge/nGe layers

The optoelectrical characterization of electrically active defects can be a very useful complementary source of information on traps in GeSn materials. The entire energy range of the bandgap can be probed, and the much lower optical capture cross sections involved give rise to longer time constants. In view of performing characterizations of GeSn layers by this method, new layers have been grown in IMEC. The goal is to illuminate the samples with light of variable energy to excite trap states within the GeSn bandgap and subsequently collect the weak electrical current resulting from the separation of those charges by the electric field in the depletion region [208, 209, 210]. The depletion region in the GeSn layer therefore needs to be relatively large.

C.1 pGeSn/n$^+$Ge/nGe layers

Samples consisting in an unintentionally p-doped GeSn layer on top of a highly n-doped Ge layer, grown on a n-Ge substrate were therefore fabricated, as schematically depicted in Fig. C.1. The Sn content in the GeSn layer was 8%. The high n-type doping of the Ge interlayer aimed at generating as large a depletion region in the GeSn layer as possible, while reducing its width on the Ge side.

After growth, the thickness of the GeSn layer was measured to be between 220 and 250 nm, the Phosphorus doped Ge layer was 257 nm thick and the thickness of the Ge substrate was 450 µm.

Fig. C.2 shows the simulated total carrier concentration, comprising both holes and electrons as a function of position from the top of the sample.

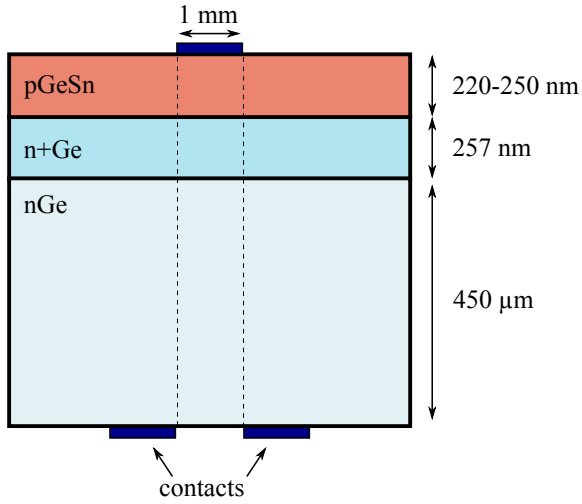


Figure C.1: Unscaled schematic of the pGeSn/n$^+$Ge/nGe samples grown for optoelectrical characterization. A round top contact of Al with 1 mm diameter is deposited, and a circular backcontact is deposited on the opposite side.

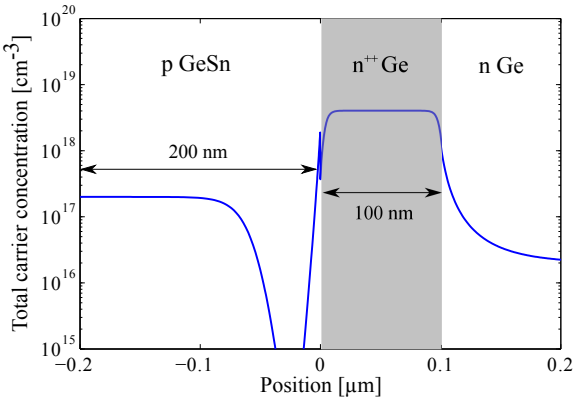


Figure C.2: Total carrier concentration $(n + p)$ as a function of position from the top GeSn layer, showing the depletion region at the pGeSn/n$^+$Ge interface.

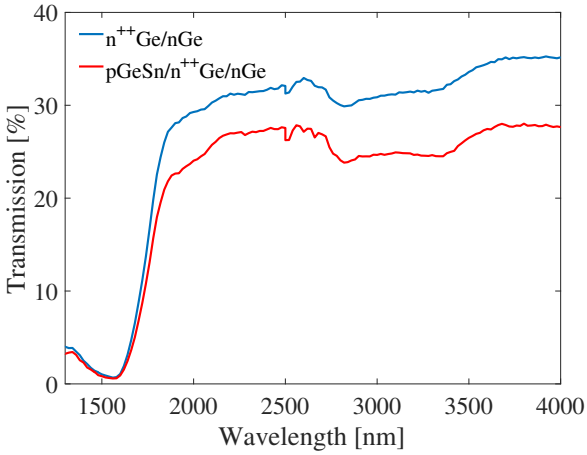


Figure C.3: Transmission spectra of the reference n$^+$Ge/nGe sample and the pGeSn/n$^+$Ge/nGe sample.

The carrier concentration in the GeSn layer has been estimated around 2×10^{17} cm^{-3} and that of the n$^+$Ge layer, 4×10^{18} cm^{-3}. The depletion region extends therefore almost up to 100 nm into the GeSn layer and can be even further expanded by the application of a reverse bias. This theoretical calculation confirms that the design of the real structure meets the device requirement exposed earlier.

C.2 Absorption

Optical absorption measurements were first performed on those samples before contact deposition, at room temperature. The light source was a 100 W halogen bulb, which was chosen because of its high emission in the near infrared (IR) range (700 nm - 2500 nm) and up to 4000 nm. A 2×2 mm PbSe photoconductive IR detector from Hamamatsu was used for the detection of the remaining light. A two-stage thermoelectric cooling inside the photodetector allows to lower its temperature down to 240 K and improve its sensitivity as well as reduce the impact of ambient noise. The semiconductor sample itself can be cooled by a computer-controlled liquid nitrogen flow in the metallic body of the sample holder. Temperatures as low as 130 K can be reached, with a stability below 1 K.

Both the absorption of a pGeSn/n$^+$Ge/nGe and a reference n$^+$Ge/nGe samples were measured from 1400 nm to 4000 nm, as shown in Fig. C.3. A

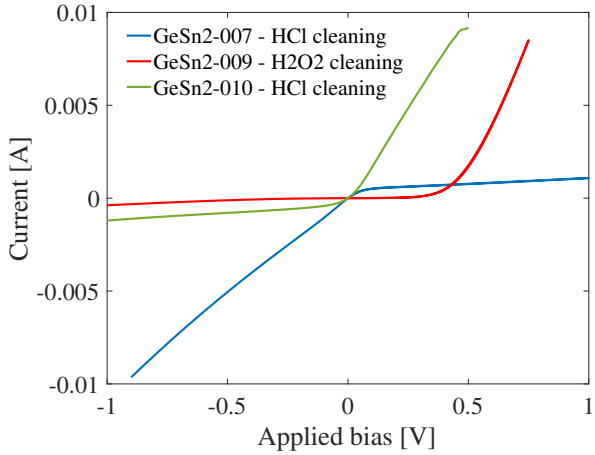


Figure C.4: I-V curves of the pGeSn/n$^+$Ge/nGe samples with various metal contact evaporation procedures: H_2O_2 or HCl cleaning and high or low heating current through the evaporated metal.

clear drop in the transmission occurs for wavelengths below 1700 nm, which corresponds to a value close to the bandgap energy of Ge. The wavelength shift between the GeSn sample and the Ge reference sample, although discernable, is very limited. It is also much less than what would be expected from the reduced bandgap of a GeSn layer with 5%.

C.3 Metal contact deposition

In order to carry out photo-electrical measurements, metal aluminum contacts were evaporated on both sides of the samples. A special two-sided deposition mask was used in order to align the center dot contact on the top GeSn layer with the annular back contact on the Ge substrate, through which the IR light will be applied (see Fig. C.1).

One of the samples, labeled GeSn2-007, was first cleaned by a 30 second dip in 50% HCl [68] then blown with dry N_2 and the metal contacts were evaporated. The I-V curve measured on those contacts, as shown in Fig. C.4, is opposite to what one would expect when biasing a pn junction. The current is indeed much lower when a positive bias is applied to the top GeSn (p-type) contact than when a negative bias is applied.

Various hypotheses were considered, but it looked like the most likely origin of this unexpected behaviour would reside in the unperfect metal

deposition that would lead to a far from ohmic contact. New contacts were therefore evaporated on a new sample, GeSn2-009, this time using a pre-cleaning procedure with H_2O_2 instead of the dilute HCl. The heating current used for the evaporation of the Al marble was also slightly increased, from 120 A to $140 - 150$ A, for a same deposition time, which is expected to result in a thicker contact deposition. The I-V characteristics of this new sample, also shown in Fig. C.4, indicates a behaviour that is reversed from the previous one, and in accordance with the theoretical comportment of a pn junction.

In order to rule out the effect of either the cleaning method or the higher heating current, a third contact deposition was performed on sample GeSn2-010 using, again, the initial HCl cleaning method and the higher heating current. The result is shown in Fig. C.4 and reveals a behaviour that is similar to that of sample GeSn2-009.

It was therefore concluded that the first measurement resulted not from the choice of cleaning method, but from the insufficient heating current. This lead to an inadequate contact thickness estimated around 80 nm which was at the origin of the reversed I-V behaviour. The next two samples, with a denser metallic contact, did not show the same issue, independently of the cleaning method used.

Appendix D

$GeSnO_2$ and GeO_2 MOS capacitors

Following the discussion of the $GeSnO_2$ and GeO_2 samples at the end of Chapter 6 (page 148), a more detailed analysis of the circuit modeling and fitting is presented in this appendix.

Starting with the $GeSnO_2$ sample, various equivalent electrical circuit models have been envisioned. The most simple one, corresponding to an ideal MOS capacitor, corresponds to a pure capacitance accounting for the oxide, in series with a parallel RC couple for the depletion region. This model would imply that the resistance at low frequency should tend to infinity, which is obviously not the case, as demonstrated by the experimental data shown in Fig. D.2. The high frequency resistance is also not zero, which indicates the presence of a series resistance from the bulk of the device, which remains present when the resistive parts of both the depletion and the oxide regions are shorted at high frequency by their reactive counterparts (the capacitors). The first model that has therefore been considered for fitting to the experimental data is that of Fig. D.1 (a). Figure D.2 shows the result of this fit, where it can be seen that the general trend of the experimental data is matched, with the presence of the two main plateaus in the R curve. The accuracy of the fitting could clearly be improved, though.

A more complex model has subsequently been considered, involving a series combination of a resistor a capacitor in parallel with the depletion elements (Fig. D.1 (b)). The addition of this RC couple, with a time constant τ =RC, is intended to account for the presence of traps in the model [111]. The result of the fit, shown in Fig. D.3, demonstrates a clear improvement over the previous model.

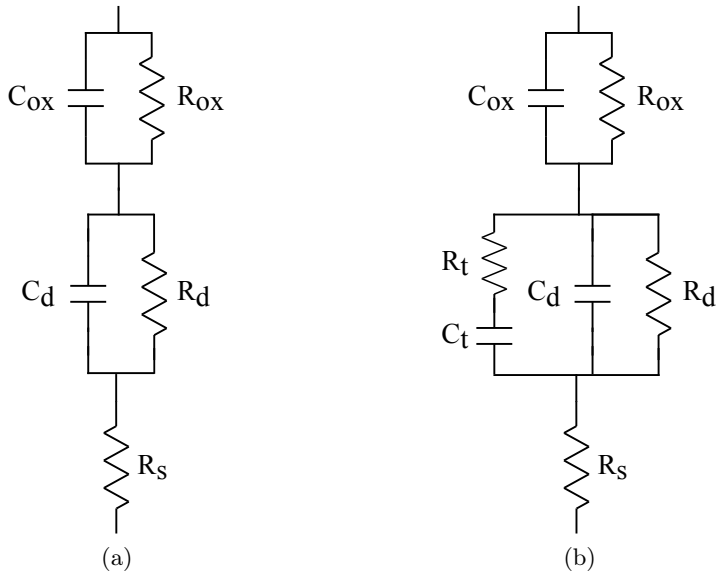


Figure D.1: Equivalent circuit model of the MOS structure (a) with conduction through the oxide and a series resistance and (b) with the addition of a series RC couple to account for the presence of a trap.

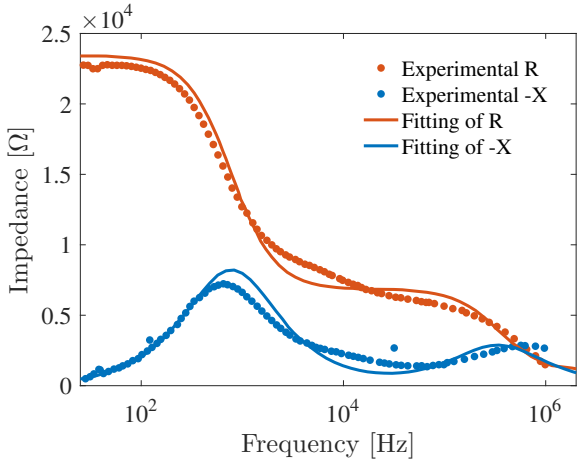


Figure D.2: Fitting of a double RC with a series resistance circuit model (no traps included) to the impedance spectrum of the $GeSnO_2$ sample at 90 K and 0 V.

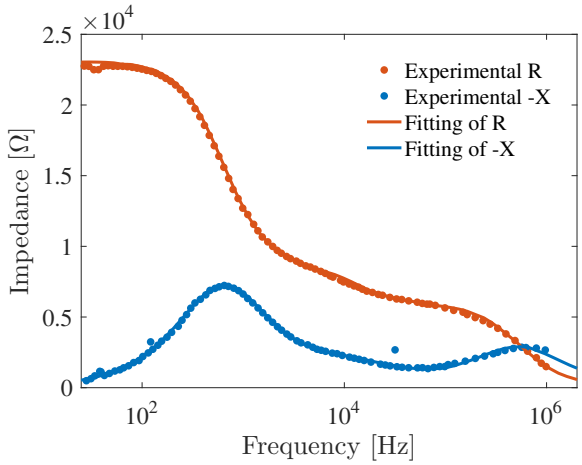


Figure D.3: Fitting of a double RC with a series resistance circuit model, with an additional RC couple to account for a trap level (Fig. D.1 (b)), to the impedance spectrum of the $GeSnO_2$ sample at 90 K and 0 V.

In order to gain more insight into the relative influence of the various elements of this electrical model, their contributions have been separated into the sum of the oxide impedance (R_{oxide} and X_{oxide}), the depletion and trap impedance ($R_{depl+trap}$ and $X_{depl+trap}$) and the series resistance R_S. These contributions are displayed in Fig. D.4. At low frequency, the total resistance is basically the sum of the oxide, depletion+trap and series resistance $R_{oxide}+R_{depl+trap}+R_S$. Indeed at low frequency, the impedance of the branch related to the traps increases to a very high value because of its reactive part and is therefore dominated by the parallel R_{depl} resistor.

As compared to the model of Fig. D.1 (a), however, the cut-off frequency of the depletion region is impacted by the presence of the traps. The admittance of the depletion/trap region is

$$Y_{depl+trap} = Y_{depl}+Y_{trap} = \left[\frac{1}{R_{depl}} + \frac{C_{trap}\omega^2\tau_{trap}}{1+\omega^2\tau_{trap}^2}\right] + j\omega\left[C_{depl} + \frac{C_{trap}}{1+\omega^2\tau_{trap}^2}\right] \tag{D.1}$$

with $\tau_{trap} = C_{trap}R_{trap}$. Depending on the measurement frequency ω, the equivalent capacitance of the depletion/trap combination is therefore

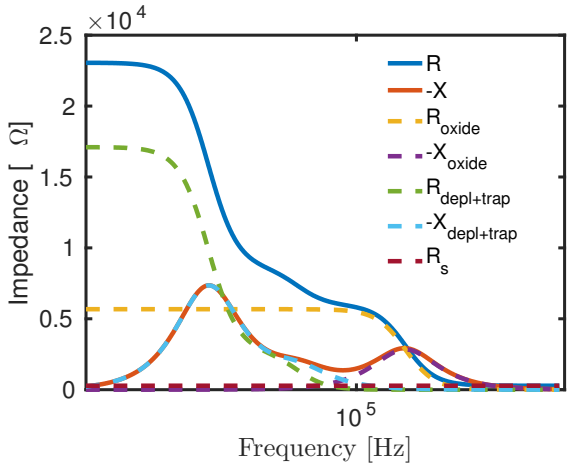


Figure D.4: Comparison of the contributions of the oxide and depletion impedances to the total impedance of the $GeSnO_2$ sample.

$$C_{\text{depl+trap}} = \begin{cases} C_{\text{depl}} + C_{\text{trap}} & \text{if } \omega \ll 1/\tau_{\text{trap}} \\ C_{\text{depl}} + C_{\text{trap}}/2 & \text{if } \omega = 1/\tau_{\text{trap}} \\ C_{\text{depl}} & \text{if } \omega \gg 1/\tau_{\text{trap}}. \end{cases} \tag{D.2}$$

From the fitting of the model to the experimental data, a time constant $\tau_{\text{trap}} = 4.8 \times 10^{-5}$ s is obtained, which leads to a cutoff frequency $f_c = 3.3$ kHz.

The two models from Fig. D.1 (a) and (b) have also been fitted to the experimental data of the GeO_2 sample. Figure D.5 shows the first fit, including only two parallel RC couples and a series resistance. The fit is seen to be very good already, even though no trap is considered in the model. This is consistent with the observation that a much lower density of traps is expected to be present, based on other measurements, such as IV and DLTS.

With the addition of a RC couple to take into account a trap level, the fit improves substantially, as shown in Fig. D.6. This improvement is nowhere as dramatic as for the $GeSnO_2$ sample, though, which again tends to confirm the lower density of traps in this sample.

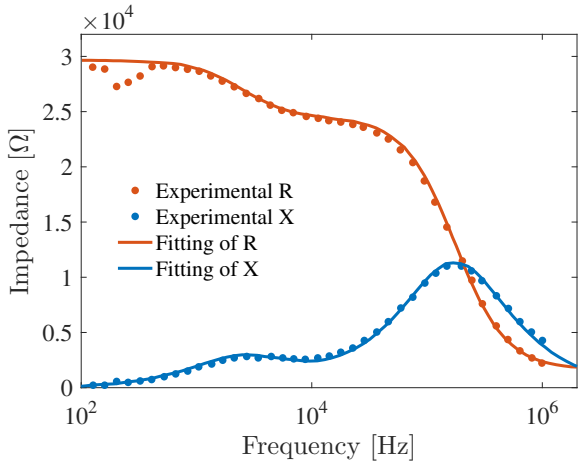


Figure D.5: Fitting of a double RC with a series resistance circuit model to the impedance spectrum of the GeO_2 sample at 90 K and 0 V.

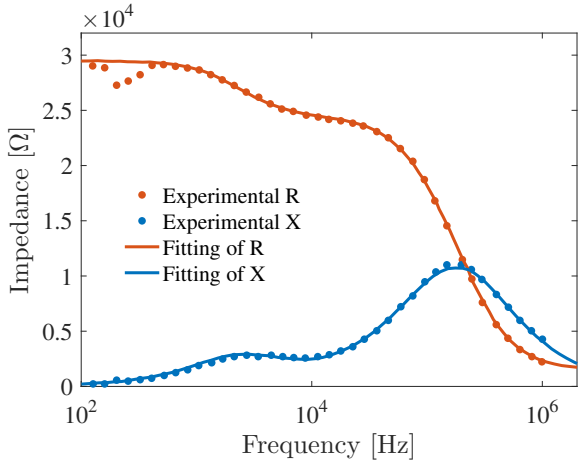


Figure D.6: Fitting of a double RC with a series resistance circuit model, with an additional RC couple to account for a trap level (Fig. D.1 (b)), to the impedance spectrum of the GeO_2 sample at 90 K and 0 V.

Bibliography

[1] GA Busch and R Kebn. Semiconducting properties of gray tin. *Solid State Physics*, 11:1–40, 1960.

[2] FA Trumbore. Solid solubilities and electrical properties of tin in germanium single crystals. *Journal of the Electrochemical society*, 103(11):597–600, 1956.

[3] CD Thurmond, FA Trumbore, and M Kowalchik. Germanium solidus curves. *The Journal of Chemical Physics*, 25(4):799–800, 1956.

[4] Richard Soref, John Kouvetakis, John Tolle, Jose Menendez, and Vijay D'Costa. Advances in SiGeSn technology. *Journal of Materials Research*, 22(12):3281–3291, 2007.

[5] Robert H Dennard, Fritz H Gaensslen, V Leo Rideout, Ernest Bassous, and Andre R LeBlanc. Design of ion-implanted MOSFET's with very small physical dimensions. *IEEE Journal of Solid-State Circuits*, 9(5):256–268, 1974.

[6] Gordon Moore. Cramming More Components Onto Integrated Circuits, Electronics,(38) 8, 1965.

[7] S Natarajan, M Agostinelli, S Akbar, M Bost, A Bowonder, V Chikarmane, S Chouksey, A Dasgupta, K Fischer, Q Fu, et al. A 14nm logic technology featuring 2 nd-generation FinFET, air-gapped interconnects, self-aligned double patterning and a 0.0588 μm 2 SRAM cell size. In *2014 IEEE International Electron Devices Meeting*, pages 3–7. IEEE, 2014.

[8] Yanning Sun, SJ Koester, EW Kiewra, JP de Souza, N Ruiz, JJ Bucchignano, A Callegari, KE Fogel, DK Sadana, J Fompeyrine, et al. Post-Si CMOS: III-V n-MOSFETs with high-k gate dielectrics. In *Compound Semiconductor Integrated Circuit Symposium*, 2007.

[9] Edward J Nowak. Maintaining the benefits of CMOS scaling when scaling bogs down. *IBM Journal of Research and Development*, 46(2.3):169–180, 2002.

[10] Juan-Antonio Carballo, Wei-Ting Jonas Chan, Paolo A Gargini, Andrew B Kahng, and Siddhartha Nath. ITRS 2.0: Toward a re-framing of the Semiconductor Technology Roadmap. In *2014 IEEE 32nd International Conference on Computer Design (ICCD)*, pages 139–146. IEEE, 2014.

[11] Bill Chen, Bill Bottoms, Dave Armstrong, and Atsunobu Isobayashi. ITRS 2.0: Heterogeneous Integration. *SOLID STATE TECHNOLOGY*, 58(3):13–17, 2015.

[12] IEEE Rebooting Computing Initiative, Standards Association, and Computer Society Introduce New International Roadmap for Devices and Systems to Set the Course for End-to-End Computing. `http://rebootingcomputing.ieee.org/images/files/pdf/rc_irds.pdf`. Accessed: 2016-07-20.

[13] Shigeaki Zaima. Technology Evolution for Silicon Nanoelectronics: Postscaling Technology. *Japanese Journal of Applied Physics*, 52(3R):030001, March 2013.

[14] Xuejue Huang, Wen-Chin Lee, Charles Kuo, Digh Hisamoto, Leland Chang, Jakub Kedzierski, Erik Anderson, Hideki Takeuchi, Yang-Kyu Choi, Kazuya Asano, et al. Sub 50-nm finfet: Pmos. In *Electron Devices Meeting, 1999. IEDM'99. Technical Digest. International*, pages 67–70. IEEE, 1999.

[15] Mitsumasa Koyanagi, Hiroyuki Kurino, Kang Wook Lee, Katsuyuki Sakuma, Nobuaki Miyakawa, and Hikotaro Itani. Future system-on-silicon LSI chips. *Ieee Micro*, 18(4):17–22, 1998.

[16] Satoshi Sugahara and Masaaki Tanaka. A spin metal–oxide–semiconductor field-effect transistor using half-metallic-ferromagnet contacts for the source and drain. *Applied Physics Letters*, 84(13):2307–2309, 2004.

[17] Martin Gajek, Manuel Bibes, Stephane Fusil, Karim Bouzehouane, Josep Fontcuberta, Agnes Barthelemy, and Albert Fert. Tunnel junctions with multiferroic barriers. *Nature materials*, 6(4):296–302, 2007.

[18] Tahir Ghani, Michael Armstrong, Chris Auth, M Bost, P Charvat, G Glass, T Hoffmann, K Johnson, C Kenyon, J Klaus, et al. A 90nm high volume manufacturing logic technology featuring novel 45nm gate length strained silicon CMOS transistors. In *Electron Devices Meeting, 2003. IEDM'03 Technical Digest. IEEE International*, pages 11–6. IEEE, 2003.

[19] Friedrich Schäffler. High-mobility Si and Ge structures. *Semiconductor Science and Technology*, 12(12):1515, 1997.

[20] Benjamin Vincent, Federica Gencarelli, Hugo Bender, Clement Merckling, Bastien Douhard, Dirch Hjorth Petersen, Ole Hansen, HH Henrichsen, Johan Meersschaut, Wilfried Vandervorst, et al. Undoped and in-situ B doped GeSn epitaxial growth on Ge by atmospheric pressure-chemical vapor deposition. *Applied Physics Letters*, 99(15):152103, 2011.

[21] Shotaro Takeuchi, Yosuke Shimura, Osamu Nakatsuka, Shigeaki Zaima, Masaki Ogawa, and Akira Sakai. Growth of highly strain-relaxed Ge1-xSnx/virtual Ge by a Sn precipitation controlled compositionally step-graded method. *Applied Physics Letters*, 92(23):231916, 2008.

[22] Dieter K Schroder. *Semiconductor material and device characterization*. John Wiley & Sons, 2006.

[23] DV Lang. Deep-level transient spectroscopy: A new method to characterize traps in semiconductors. *Journal of Applied Physics*, 45(7):3023–3032, 1974.

[24] S Weiss and R Kassing. Deep Level Transient Fourier Spectroscopy (DLTFS)—A technique for the analysis of deep level properties. *Solid-State Electronics*, 31(12):1733–1742, 1988.

[25] NM Johnson. Measurement of semiconductor–insulator interface states by constant-capacitance deep-level transient spectroscopy. *Journal of Vacuum Science & Technology*, 21(2):303–314, 1982.

[26] Kimiyoshi Yamasaki, Minoru Yoshida, and Takuo Sugano. Deep level transient spectroscopy of bulk traps and interface states in Si MOS diodes. *Japanese Journal of Applied Physics*, 18(1):113, 1979.

[27] Eddy Simoen, Benjamin Vincent, Clement Merckling, Federica Gencarelli, Lung-Ku Chu, and Roger Loo. Deep-Level Transient Spec-

troscopy of MOS Capacitors on GeSn Epitaxial Layers. *ECS Transactions*, 50(5):279–287, 2013.

[28] Somya Gupta, Eddy Simoen, Roger Loo, Oreste Madia, Dennis Lin, Clement Merckling, Yosuke Shimura, Thierry Conard, Johan Lauwaert, Henk Vrielinck, et al. Density and capture cross-sections of interface traps in GeSnO2 and GeO2 grown on hetero-epitaxial GeSn. *ACS applied materials & interfaces*, 2016.

[29] S. Gupta, E. Simoen, H. Vrielinck, C. Merckling, B. Vincent, F. Gencarelli, R. Loo, and M. Heyns. Identification of Deep Levels Associated with Extended and Point Defects in GeSn Epitaxial Layers Using DLTs. *ECS Transactions*, 53(1):251–258, May 2013.

[30] Shigeaki Zaima, Osamu Nakatsuka, Noriyuki Taoka, Masashi Kurosawa, Wakana Takeuchi, and Mitsuo Sakashita. Growth and applications of GeSn-related group-IV semiconductor materials. *Science and Technology of Advanced Materials*, 2016.

[31] RW Olesinski and GJ Abbaschian. The Ge- Sn (Germanium- Tin) system. *Bulletin of Alloy Phase Diagrams*, 5(3):265–271, 1984.

[32] Shotaro Takeuchi, Akira Sakai, Koji Yamamoto, Osamu Nakatsuka, Masaki Ogawa, and Shigeaki Zaima. Growth and structure evaluation of strain-relaxed Ge1- xSnx buffer layers grown on various types of substrates. *Semiconductor science and technology*, 22(1):S231, 2006.

[33] Shotaro Takeuchi, Akira Sakai, Osamu Nakatsuka, Masaki Ogawa, and Shigeaki Zaima. Tensile strained Ge layers on strain-relaxed Ge 1- x Sn x/virtual Ge substrates. *Thin Solid Films*, 517(1):159–162, 2008.

[34] Kimihiko Kato, Takanori Asano, Noriyuki Taoka, Mitsuo Sakashita, Wakana Takeuchi, Osamu Nakatsuka, and Shigeaki Zaima. Robustness of Sn precipitation during thermal oxidation of Ge1- xSnx on Ge (001). *Japanese Journal of Applied Physics*, 53(8S1):08LD04, 2014.

[35] AY Cho and JR Arthur. Molecular beam epitaxy. *Progress in solid state chemistry*, 10:157–191, 1975.

[36] John R Arthur. Molecular beam epitaxy. *Surface science*, 500(1):189–217, 2002.

[37] PR Pukite, Alex Harwit, and SS Iyer. Molecular beam epitaxy of metastable, diamond structure SnxGe1- x alloys. *Applied Physics Letters*, 54(21):2142–2144, 1989.

[38] MT Asom, EA Fitzgerald, AR Kortan, B Spear, and LC Kimerling. Epitaxial growth of metastable SnGe alloys. *Applied Physics Letters*, 55(6):578–579, 1989.

[39] J Piao, R Beresford, T Licata, WI Wang, and H Homma. Molecular-beam epitaxial growth of metastable Ge1- xSnx alloys. *Journal of Vacuum Science & Technology B*, 8(2):221–226, 1990.

[40] PA Maksym and J L_ Beeby. A theory of RHEED. *Surface Science*, 110(2):423–438, 1981.

[41] T Franke, P Kreutzer, Th Zacher, W Naumann, and R Anton. In situ RHEED, AFM, and REM investigations of the surface recovery of MBE-grown GaAs (001)-layers during growth interruptions. *Journal of crystal growth*, 193(4):451–459, 1998.

[42] K Ploog and A Fischer. In situ characterization of MBE grown GaAs and Al x Ga1- x As films using RHEED, SIMS, and AES techniques. *Applied physics*, 13(2):111–121, 1977.

[43] Masamichi Akazawa and Hideki Hasegawa. MBE growth and in situ XPS characterization of silicon interlayers on (111) B surfaces for passivation of GaAs quantum wire devices. *Journal of Crystal Growth*, 301:951–954, 2007.

[44] G Grenet, E Bergignat, M Gendry, M Lapeyrade, and G Hollinger. In situ XPS investigation of indium surface segregation for Ga 1- x In x As and Al 1- x In x As alloys grown by MBE on InP (001). *Surface science*, 352:734–739, 1996.

[45] Gang He and Harry A Atwater. Synthesis of epitaxial SnxGe1- x alloy films by ion-assisted molecular beam epitaxy. *Applied physics letters*, 68(5):664–666, 1996.

[46] Sung-Yong Chung, Niu Jin, Anthony T Rice, Paul R Berger, Ronghua Yu, ZQ Fang, and Phillip E Thompson. Growth temperature and dopant species effects on deep levels in Si grown by low temperature molecular beam epitaxy. *Journal of applied physics*, 93(11):9104–9110, 2003.

[47] E Kasper, M Kittler, M Oehme, and T Arguirov. Germanium tin: silicon photonics toward the mid-infrared [Invited]. *Photonics Research*, 1(2):69–76, 2013.

[48] Michael L Hitchman and Klavs F Jensen. *Chemical vapor deposition: principles and applications*. Elsevier, 1993.

[49] Jong-Hee Park and TS Sudarshan. *Chemical vapor deposition*, volume 2. ASM international, 2001.

[50] Jennifer Taraci, John Tolle, John Kouvetakis, MR McCartney, David J Smith, Jose Menendez, and MA Santana. Simple chemical routes to diamond-cubic germanium-tin alloys. *Applied Physics Letters*, 78(23):3607–3609, 2001.

[51] M Bauer, J Taraci, J Tolle, AVG Chizmeshya, S Zollner, David J Smith, Jose Menendez, Changwu Hu, and John Kouvetakis. Ge–Sn semiconductors for band-gap and lattice engineering. *Applied physics letters*, 81(16):2992–2994, 2002.

[52] F. Gencarelli, B. Vincent, L. Souriau, O. Richard, W. Vandervorst, R. Loo, M. Caymax, and M. Heyns. Low-temperature Ge and GeSn Chemical Vapor Deposition using Ge2H6. *Thin Solid Films*, 520(8):3211–3215, February 2012.

[53] Y Chibane and M Ferhat. Electronic structure of SnxGe1- x alloys for small Sn compositions: Unusual structural and electronic properties. *Journal of Applied Physics*, 107(5):053512, 2010.

[54] Vijay R D'Costa, Candi S Cook, AG Birdwell, Chris L Littler, Michael Canonico, Stefan Zollner, John Kouvetakis, and José Menéndez. Optical critical points of thin-film Ge 1- y Sn y alloys: a comparative Ge 1- y Sn y/ Ge 1- x Si x study. *Physical Review B*, 73(12):125207, 2006.

[55] Yosuke Shimura, Wei Wang, Thomas Nieddu, Federica Gencarelli, Benjamin Vincent, Priya Laha, Herman Terryn, Stefan Stefanov, Stefano Chiussi, Joris Van Campenhout, et al. Bandgap Measurement by Spectroscopic Ellipsometry for Strained Ge1-xSnx. *8th Int. Conf. on Si epitaxy and Heterostructures (ICSI-8), Book of Abstracts*, page 65, 2013.

[56] Gang He and Harry A Atwater. Interband transitions in Sn x Ge 1- x alloys. *Physical review letters*, 79(10):1937, 1997.

[57] H Pérez Ladrón de Guevara, AG Rodrıguez, H Navarro-Contreras, and MA Vidal. Determination of the optical energy gap of Ge1- xSnx alloys with 0< x< 0.14. *Applied Physics Letters*, 84(22):4532–4534, 2004.

[58] J Mathews, RT Beeler, J Tolle, C Xu, R Roucka, John Kouvetakis, and J Menéndez. Direct-gap photoluminescence with tunable emission wavelength in Ge 1- y Sn y alloys on silicon. *Appl. Phys. Lett*, 97:221912, 2010.

[59] Robert Chen, Hai Lin, Yijie Huo, Charles Hitzman, Theodore I Kamins, and James S Harris. Increased photoluminescence of strain-reduced, high-Sn composition Ge1- xSnx alloys grown by molecular beam epitaxy. *Applied Physics Letters*, 99(18):181125, 2011.

[60] G Grzybowski, RT Beeler, L Jiang, DJ Smith, John Kouvetakis, and Jose Menendez. Next generation of Ge1- ySny (y= 0.01-0.09) alloys grown on Si (100) via Ge3H8 and SnD4: Reaction kinetics and tunable emission. *Applied Physics Letters*, 101(7):072105, 2012.

[61] Suyog Gupta, Blanka Magyari-Köpe, Yoshio Nishi, and Krishna C Saraswat. Achieving direct band gap in germanium through integration of Sn alloying and external strain. *Journal of Applied Physics*, 113(7):073707, 2013.

[62] Lars Vegard. Die konstitution der mischkristalle und die raumfüllung der atome. *Zeitschrift für Physik A Hadrons and Nuclei*, 5(1):17–26, 1921.

[63] Richard Dalven. Empirical relation between energy gap and lattice constant in cubic semiconductors. *Physical Review B*, 8(12):6033, 1973.

[64] J Kouvetakis, Jose Menendez, and AVG Chizmeshya. Tin-based group IV semiconductors: New platforms for opto-and microelectronics on silicon. *Annu. Rev. Mater. Res.*, 36:497–554, 2006.

[65] R Beeler, R Roucka, AVG Chizmeshya, J Kouvetakis, and J Menéndez. Nonlinear structure-composition relationships in the Ge 1- y Sn y/Si (100)(y< 0.15) system. *Physical Review B*, 84(3):035204, 2011.

[66] Su Shao-Jian, Cheng Bu-Wen, Xue Chun-Lai, Zhang Dong-Liang, Zhang Guang-Ze, and Wang Qi-Ming. Lattice constant deviation from Vegard's law in GeSn alloys. 2012.

[67] Federica Gencarelli. Epitaxial Growth of GeSn Compounds for Advanced CMOS and PhotonicsApplications. 2015.

[68] Suyog Gupta. *Germanium-Tin (GeSn) Technology.* PhD thesis, STANFORD UNIVERSITY, 2013.

[69] Kiyohito Morii, Takashi Iwasaki, Ryosho Nakane, Mitsuru Takenaka, and Shinichi Takagi. High performance GeO 2/Ge nMOSFETs with source/drain junctions formed by gas phase doping. In *2009 IEEE International Electron Devices Meeting (IEDM)*, pages 1–4. IEEE, 2009.

[70] CH Lee, T Nishimura, T Tabata, SK Wang, K Nagashio, K Kita, and A Toriumi. Ge MOSFETs performance: Impact of Ge interface passivation. In *Electron Devices Meeting (IEDM), 2010 IEEE International*, pages 18–1. IEEE, 2010.

[71] Jerome Mitard, C Shea, Brice DeJaeger, Andrea Pristera, Gang Wang, Michel Houssa, Geert Eneman, Geert Hellings, W-E Wang, JC Lin, et al. Impact of EOT scaling down to 0.85 nm on 70nm Ge-pFETs technology with STI. In *2009 Symposium on VLSI Technology*, pages 82–83. IEEE, 2009.

[72] Tejas Krishnamohan, Donghyun Kim, Thanh Viet Dinh, Anh-tuan Pham, Bernd Meinerzhagen, Christoph Jungemann, and Krishna Saraswat. Comparison of (001),(110) and (111) uniaxial-and biaxial-strained-Ge and strained-Si PMOS DGFETs for all channel orientations: Mobility enhancement, drive current, delay and off-state leakage. In *2008 IEEE International Electron Devices Meeting*, pages 1–4. IEEE, 2008.

[73] Dimitri A Antoniadis and Ali Khakifirooz. MOSFET performance scaling: Limitations and future options. In *2008 IEEE International Electron Devices Meeting*, 2008.

[74] Masaharu Kobayashi, Jérôme Mitard, Toshifumi Irisawa, Thomas-Y Hoffmann, Marc Meuris, Krishna Saraswat, Yoshio Nishi, and Marc Heyns. On the high-field transport and uniaxial stress effect in Ge PFETs. *IEEE Transactions on Electron Devices*, 58(2):384–391, 2011.

[75] S Takagi, T Tezuka, T Irisawa, S Nakaharai, T Numata, K Usuda, N Sugiyama, M Shichijo, R Nakane, and S Sugahara. Device structures and carrier transport properties of advanced CMOS using high mobility channels. *Solid-State Electronics*, 51(4):526–536, 2007.

[76] DL Rode. Electron transport in InSb, InAs, and InP. *Physical Review B*, 3(10):3287, 1971.

[77] Tomonori Nishimura, Choong Hyun Lee, Toshiyuki Tabata, Sheng Kai Wang, Kosuke Nagashio, Koji Kita, and Akira Toriumi. High-

Electron-Mobility Ge n-Channel Metal–Oxide–Semiconductor Field-Effect Transistors with High-Pressure Oxidized Y2O3. *Applied physics express*, 4(6):064201, 2011.

[78] Max V Fischetti and Steven E Laux. Band structure, deformation potentials, and carrier mobility in strained Si, Ge, and SiGe alloys. *Journal of Applied Physics*, 80(4):2234–2252, 1996.

[79] Julius Hållstedt. Integration of epitaxial SiGe (C) layers in advanced CMOS devices. 2007.

[80] Grace Huiqi Wang, Eng-Huat Toh, Xincai Wang, Debbie Hwee Leng Seng, Sudhinrajan Tripathy, Thomas Osipowicz, Tau Kuei Chan, Keat Mun Hoe, S Balakumar, Chih Hang Tung, et al. Silicon-Germanium-Tin (SiGeSn) Source and Drain Stressors formed by Sn Implant and Laser Annealing for Strained Silicon-Germanium Channel P-MOSFETs. In *2007 IEEE International Electron Devices Meeting*, pages 131–134. IEEE, 2007.

[81] Jay Deep Sau and Marvin L Cohen. Possibility of increased mobility in Ge-Sn alloy system. *Physical Review B*, 75(4):045208, 2007.

[82] Suyog Gupta, Robert Chen, Blanka Magyari-Kope, Hai Lin, Bin Yang, Aneesh Nainani, Yoshio Nishi, James S Harris, and Krishna C Saraswat. GeSn technology: extending the Ge electronics roadmap. In *Electron Devices Meeting (IEDM), 2011 IEEE International*, pages 16–6. IEEE, 2011.

[83] Genquan Han, Shaojian Su, Chunlei Zhan, Qian Zhou, Yue Yang, Lanxiang Wang, Pengfei Guo, Wang Wei, Choun Pei Wong, Ze Xiang Shen, et al. High-mobility germanium-tin (GeSn) p-channel MOSFETs featuring metallic source/drain and sub-370 C process modules. In *Electron Devices Meeting (IEDM), 2011 IEEE International*, pages 16–7. IEEE, 2011.

[84] Yosuke Shimura, Norimasa Tsutsui, Osamu Nakatsuka, Akira Sakai, and Shigeaki Zaima. Low temperature growth of Ge 1- x Sn x buffer layers for tensile–strained Ge layers. *Thin Solid Films*, 518(6):S2–S5, 2010.

[85] YY Fang, J Tolle, R Roucka, Andrew Chizmeshya, John Kouvetakis, VR D'Costa, and Joś Meńndez. Perfectly tetragonal, tensile-strained Ge on Ge 1-y Sn y buffered Si (100). *Applied physics letters*, 90(6), 2007.

[86] Shigeaki Zaima, Osamu Nakatsuka, Yosuke Shimura, and Shotaro Takeuchi. Tensile-strained Ge and Ge 1- x Sn x layers for high-mobility channels in future CMOS Devices. In *Solid-State and Integrated Circuit Technology (ICSICT), 2010 10th IEEE International Conference on*, pages 871–874. IEEE, 2010.

[87] Suyog Gupta, Benjamin Vincent, DHC Lin, M Gunji, Andrea Firrincieli, Federica Gencarelli, B Magyari-Köpe, B Yang, Bastien Douhard, Joris Delmotte, et al. GeSn channel nMOSFETs: Material potential and technological outlook. In *VLSI Technology (VLSIT), 2012 Symposium on*, pages 95–96. IEEE, 2012.

[88] Genquan Han, Shaojian Su, Lanxiang Wang, Wei Wang, Xiao Gong, Yue Yang, Pengfei Guo, Cheng Guo, Guangze Zhang, Jisheng Pan, et al. Strained germanium-tin (GeSn) N-channel MOSFETs featuring low temperature N+/P junction formation and GeSnO2 interfacial layer. In *VLSI Technology (VLSIT), 2012 Symposium on*, pages 97–98. IEEE, 2012.

[89] Jay Mathews, Radek Roucka, Junqi Xie, Shui-Qing Yu, José Menéndez, and John Kouvetakis. Extended performance GeSn/Si (100) pin photodetectors for full spectral range telecommunication applications. *Applied Physics Letters*, 95(13):133506, 2009.

[90] J Werner, M Oehme, A Schirmer, E Kasper, and J Schulze. Molecular beam epitaxy grown GeSn pin photodetectors integrated on Si. *Thin Solid Films*, 520(8):3361–3364, 2012.

[91] Shaojian Su, Buwen Cheng, Chunlai Xue, Wei Wang, Quan Cao, Haiyun Xue, Weixuan Hu, Guangze Zhang, Yuhua Zuo, and Qiming Wang. GeSn pin photodetector for all telecommunication bands detection. *Optics express*, 19(7):6400–6405, 2011.

[92] Alban Gassenq, Federica Gencarelli, Joris Van Campenhout, Yosuke Shimura, Roger Loo, G Narcy, Benjamin Vincent, and Günther Roelkens. GeSn/Ge heterostructure short-wave infrared photodetectors on silicon. *Optics express*, 20(25):27297–27303, 2012.

[93] Michael Oehme, Konrad Kostecki, Tzanimir Arguirov, Gregor Mussler, Kaiheng Ye, Martin Gollhofer, Marc Schmid, Mathias Kaschel, Roman Alexander Körner, Martin Kittler, et al. GeSn heterojunction LEDs on Si substrates. *IEEE Photonics Technology Letters*, 26(2):187–189, 2014.

[94] Shu-Wei Chang and Shun Lien Chuang. Theory of Optical Gain of Ge-Si x Ge y Sn 1- x- y Quantum-Well Lasers. *IEEE Journal of Quantum Electronics*, 43(3):249–256, 2007.

[95] Greg Sun, HH Cheng, Jose Menendez, Jacob B Khurgin, and RA Soref. Strain-free Ge/GeSiSn quantum cascade lasers based on L-valley intersubband transitions. 2007.

[96] Yuan-Hui Zhu, Qiang Xu, Wei-Jun Fan, and Jian-Wei Wang. Theoretical gain of strained GeSn0. 02/Ge1-x-y'SixSny'quantum well laser. *Journal of Applied Physics*, 107(7):3108, 2010.

[97] G Sun, RA Soref, and HH Cheng. Design of an electrically pumped SiGeSn/GeSn/SiGeSn double-heterostructure midinfrared laser. *Journal of Applied Physics*, 108(3):033107, 2010.

[98] Guo-En Chang, Shu-Wei Chang, and Shun Lien Chuang. Strain-balanced multiple-quantum-well lasers. *IEEE journal of Quantum Electronics*, 46(12):1813–1820, 2010.

[99] Stephan Wirths, R Geiger, N Von Den Driesch, G Mussler, T Stoica, S Mantl, Z Ikonic, Ml Luysberg, S Chiussi, JM Hartmann, et al. Lasing in direct-bandgap GeSn alloy grown on Si. *Nature photonics*, 9(2):88–92, 2015.

[100] Yan-Yan Fang, Junqi Xie, John Tolle, Radek Roucka, Vijay R D'Costa, Andrew VG Chizmeshya, Jose Menendez, and John Kouvetakis. Molecular-based synthetic approach to new group IV materials for high-efficiency, low-cost solar cells and Si-based optoelectronics. *Journal of the American Chemical Society*, 130(47):16095–16102, 2008.

[101] VR D'Costa, YY Fang, J Tolle, John Kouvetakis, and Jose Menendez. Direct absorption edge in GeSiSn alloys. In *29th International Conference on Physics of Semiconductors, ICPS 29*, 2009.

[102] John Wilfred Orton and Peter Blood. The electrical characterization of semiconductors: measurement of minority carrier properties. *Techniques of physics*, (13), 1990.

[103] William Shockley. The Theory of p-n Junctions in Semiconductors and p-n Junction Transistors. *Bell System Technical Journal*, 28(3):435–489, 1949.

[104] Hans Albrecht Bethe. *Theory of the boundary layer of crystal rectifiers*. Radiation Laboratory, Massachusetts Institute of Technology, 1942.

[105] CR Crowell and SM Sze. Electron-optical-phonon scattering in the emitter and collector barriers of semiconductor-metal-semiconductor structures. *Solid-State Electronics*, 8(12):979–990, 1965.

[106] Chung-Whei Kao, C Lawrence Anderson, and CR Crowell. Photoelectron injection at metal-semiconductor interfaces. *Surface Science*, 95(1):321–339, 1980.

[107] CR Crowell and SM Sze. Current transport in metal-semiconductor barriers. *Solid-state electronics*, 9(11):1035–1048, 1966.

[108] CR Crowell and SM Sze. Quantum-Mechanical Reflection of Electrons at Metal-Semiconductor Barriers: Electron Transport in Semiconductor-Metal-Semiconductor Structures. *Journal of Applied Physics*, 37(7):2683–2689, 1966.

[109] CY Chang and SM Sze. Carrier transport across metal-semiconductor barriers. *Solid-State Electronics*, 13(6):727–740, 1970.

[110] Chih-Tang Sah, Robert Noyce, and William Shockley. Carrier generation and recombination in pn junctions and pn junction characteristics. *Proceedings of the IRE*, 45(9):1228–1243, 1957.

[111] Simon M Sze and Kwok K Ng. *Physics of semiconductor devices*. John wiley & sons, 1981.

[112] Sanjay Kumar Banerjee and Ben G Streetman. *Solid State Electronic Devices*. Prentice Hall, 2010.

[113] J Hilibrand and RD Gold. Determination of the impurity distribution in junction diodes from capacitance-voltage measurements. *RCA review*, 21(2):245–252, 1960.

[114] Oliver Heaviside. *Electrical papers*, volume 2. Cambridge University Press, 2011.

[115] Mirna Urquidi-Macdonald, Silvia Real, and Digby D Macdonald. Applications of Kramers—Kronig transforms in the analysis of electrochemical impedance data—III. Stability and linearity. *Electrochimica Acta*, 35(10):1559–1566, 1990.

[116] J Matthew Esteban and Mark E Orazem. On the application of the Kramers-Kronig relations to evaluate the consistency of electrochemical impedance data. *Journal of the Electrochemical Society*, 138(1):67–76, 1991.

[117] J Ross Macdonald. Impedance spectroscopy. *Annals of biomedical engineering*, 20(3):289–305, 1992.

[118] Florian Mansfeld. Electrochemical impedance spectroscopy (EIS) as a new tool for investigating methods of corrosion protection. *Electrochimica Acta*, 35(10):1533–1544, 1990.

[119] Kenneth S Cole and Robert H Cole. Dispersion and absorption in dielectrics I. Alternating current characteristics. *The Journal of Chemical Physics*, 9(4):341–351, 1941.

[120] DL Losee. Admittance spectroscopy of impurity levels in Schottky barriers. *Journal of Applied Physics*, 46(5):2204–2214, 1975.

[121] M Beguwala and CR Crowell. Characterization of multiple deep level systems in semiconductor junctions by admittance measurements. *Solid-State Electronics*, 17(2):203–214, 1974.

[122] WG Oldham and SS Naik. Admittance of p-n junctions containing traps. *Solid-State Electronics*, 15(10):1085–1096, 1972.

[123] E Schibli and AG Milnes. Effects of deep impurities on n+ p junction reverse-biased small-signal capacitance. *Solid-State Electronics*, 11(3):323–334, 1968.

[124] Eun Ji Kim, Evgueni Chagarov, Joël Cagnon, Yu Yuan, Andrew C Kummel, Peter M Asbeck, Susanne Stemmer, Krishna C Saraswat, and Paul C McIntyre. Atomically abrupt and unpinned Al2O3/In0. 53Ga0. 47As interfaces: Experiment and simulation. *Journal of Applied Physics*, 106(12):124508, 2009.

[125] S Koveshnikov, N Goel, P Majhi, H Wen, MB Santos, S Oktyabrsky, V Tokranov, R Kambhampati, R Moore, F Zhu, et al. In0. 53Ga0. 47As based metal oxide semiconductor capacitors with atomic layer deposition ZrO2 gate oxide demonstrating low gate leakage current and equivalent oxide thickness less than 1 nm. *Applied Physics Letters*, 92(22):2904, 2008.

[126] Lewis M Terman. An investigation of surface states at a silicon/silicon oxide interface employing metal-oxide-silicon diodes. *Solid-State Electronics*, 5(5):285–299, 1962.

[127] Edward H Nicollian, John R Brews, and Edward H Nicollian. *MOS (metal oxide semiconductor) physics and technology*, volume 1987. Wiley New York et al., 1982.

[128] EH Nicollian and A Goetzberger. The Si-SiO2 Interface—Electrical Properties as Determined by the Metal-Insulator-Silicon Conductance Technique. *Bell System Technical Journal*, 46(6):1055–1133, 1967.

[129] Fahrettin Yakuphanoglu. Analysis of interface states of metal–insulator–semiconductor photodiode with n-type silicon by conductance technique. *Sensors and Actuators A: Physical*, 147(1):104–109, 2008.

[130] K Lehovec. Frequency dependence of the impedance of distributed surface states in MOS structures. *Applied Physics Letters*, 8(2):48–50, 1966.

[131] K Lehovec and A Slobodskoy. Impedance of semiconductor-insulator-metal capacitors. *Solid-State Electronics*, 7(1):59–79, 1964.

[132] CGB Garrett. High-Frequency Relaxation Processes in the Field-Effect Experiment. *Physical Review*, 107(2):478, 1957.

[133] JA Cooper and RJ Schwartz. Electrical characteristics of the SiO2/Si interface near midgap and in weak inversion. *Solid-State Electronics*, 17(7):641–654, 1974.

[134] We Shockley and WT Read Jr. Statistics of the recombinations of holes and electrons. *Physical review*, 87(5):835, 1952.

[135] RDS Yadava. Analytic approach to the ac conductance method for rapid characterization of interface states in MOS structures. *Solid-state electronics*, 33(1):127–137, 1990.

[136] Roman Engel-Herbert, Yoontae Hwang, and Susanne Stemmer. Comparison of methods to quantify interface trap densities at dielectric/III-V semiconductor interfaces. *Journal of Applied Physics*, 108(12):124101, 2010.

[137] Koen Martens, Chi On Chui, Guy Brammertz, Brice De Jaeger, Duygu Kuzum, Marc Meuris, Marc M Heyns, Tejas Krishnamohan, Krishna Saraswat, Herman E Maes, et al. On the correct extraction of interface trap density of MOS devices with high-mobility semiconductor substrates. *Electron Devices, IEEE Transactions on*, 55(2):547–556, 2008.

[138] EH Nicollian, A Goetzberger, and AD Lopez. Expedient method of obtaining interface state properties from MIS conductance measurements. *Solid-State Electronics*, 12(12):937–944, 1969.

[139] B. Baert, M. Schmeits, and N.D. Nguyen. Study of the energy distribution of the interface trap density in a GeSn MOS structure by numerical simulation of the electrical characteristics. *Applied Surface Science*, 291:25–30, February 2014.

[140] Guy Brammertz, Alireza Alian, Dennis Han-Chung Lin, Marc Meuris, Matty Caymax, and W-E Wang. A Combined Interface and Border Trap Model for High-Mobility Substrate Metal–Oxide–Semiconductor Devices Applied to and InP Capacitors. *Electron Devices, IEEE Transactions on*, 58(11):3890–3897, 2011.

[141] Koen Martens. *Electrical Characterization and Modeling of Ge/III-V-Dielectric Interfaces*. PhD thesis, PhD thesis, KU Leuven, 2009.

[142] Guy Brammertz, Koen Martens, Sonja Sioncke, Annelies Delabie, Matty Caymax, Marc Meuris, and Marc Heyns. Characteristic trapping lifetime and capacitance-voltage measurements of GaAs metal-oxide-semiconductor structures. *Applied physics letters*, 91(13):133510, 2007.

[143] Kazunari Okada and Toshimasa Sekino. Impedance Measurement Handbook. *Agilent Technologies*, 128:5950–3000, 2003.

[144] Siegfried Selberherr. *Analysis and simulation of semiconductor devices*. Springer-Verlag, 1984.

[145] Karlheinz Seeger. *Semiconductor physics, An Introduction*. Springer Verlag, 1999.

[146] Charles M Wolfe, Nick Holonyak Jr, and Gregory E Stillman. *Physical properties of semiconductors*. Prentice-Hall, Inc., 1988.

[147] Walter Heywang and Hans W Pötzl. *Bänderstruktur und Stromtransport*. Springer-Verlag, 1976.

[148] Gary P Zank. The Boltzmann Transport Equation. In *Transport Processes in Space Physics and Astrophysics*, pages 71–119. Springer, 2014.

[149] W van Roosbroeck. Theory of the flow of electrons and holes in germanium and other semiconductors. *Bell System Technical Journal*, 29(4):560–607, 1950.

[150] Esther Marley Conwell. *High field transport in semiconductors*. Number 9. Academic Press, 1967.

[151] John M Ziman. *Electrons and phonons: the theory of transport phenomena in solids*. Oxford University Press, 1960.

[152] Frank J Blatt. *Physics of electronic conduction in solids*. McGraw-Hill, 1968.

[153] JM Dorkel. On electrical transport in non-isothermal semi-conductors. *Solid-state electronics*, 26(8):819–821, 1983.

[154] Juh Tzeng Lue. Theory of Schottky barrier heights of amorphous MIS solar cells. *Solid-State Electronics*, 25(9):869–874, 1982.

[155] AP Gnädinger and HE Talley. Quantum mechanical calculation of the carrier distribution and the thickness of the inversion layer of a MOS field-effect transistor. *Solid-State Electronics*, 13(9):1301–1309, 1970.

[156] SE Laux and RJ Lomax. Effect of mesh spacing on static negative resistance in GaAs MESFET simulation. *IEEE Transactions on Electron Devices*, 28(1):120–122, 1981.

[157] SE Laux. Two-dimensional simulation of GaAs MESFETS using the finite element method. 1981.

[158] GD Hachtel, MH Mack, RR O'Brien, and B Speelpenning. Semiconductor analysis using finite elements—Part I: Computational aspects. *IBM Journal of Research and Development*, 25(4):232–245, 1981.

[159] Peter A Markovich, CA Ringhofer, Erasmus Langer, and Siegfried Selberherr. An Asymptotic Anslysis of Single-Junction Semiconductor Devices. Technical report, DTIC Document, 1983.

[160] Adelaida Borisovna Vasil'eva and VG Stel'makh. Singularly disturbed systems of the theory of semiconductor devices. *USSR Computational Mathematics and Mathematical Physics*, 17(2):48–58, 1977.

[161] A De Mari. An accurate numerical steady-state one-dimensional solution of the pn junction. *Solid-State Electronics*, 11(1):33–58, 1968.

[162] A De Mari. An accurate numerical one-dimensional solution of the PN junction under arbitrary transient conditions. *Solid-State Electronics*, 11(11):1021–1053, 1968.

[163] Christian Grossmann, Hans-Görg Roos, and Martin Stynes. *Numerical treatment of partial differential equations*. Springer, 2007.

[164] Donald L Scharfetter and Hermann K Gummel. Large-signal analysis of a silicon read diode oscillator. *Electron Devices, IEEE Transactions on*, 16(1):64–77, 1969.

[165] Hermann K Gummel. A self-consistent iterative scheme for one-dimensional steady state transistor calculations. *Electron Devices, IEEE Transactions on*, 11(10):455–465, 1964.

[166] S Munnix and D Bimberg. Carrier injection in semiconductors with position-dependent band structure: Electron-beam-induced current at heterojunctions. *Journal of applied physics*, 64(5):2505–2514, 1988.

[167] Emlyn Huw Rhoderick and Richard H Williams. *Metal-semiconductor contacts*, volume 129. Clarendon Press Oxford, 1988.

[168] CR Crowell. The Richardson constant for thermionic emission in Schottky barrier diodes. *Solid-State Electronics*, 8(4):395–399, 1965.

[169] Walter L Engl, Heinz K Dirks, and Bernd Meinerzhagen. Device modeling. *Proceedings of the IEEE*, 71(1):10–33, 1983.

[170] EJ Zaluska, PA Dubock, and HA Kemhadjian. Practical 2-dimensional bipolar-transistor-analysis algorithm. *Electronics Letters*, 25(9):599–600, 1973.

[171] Endre Süli and David F Mayers. *An introduction to numerical analysis*. Cambridge university press, 2003.

[172] James M Ortega and Werner C Rheinboldt. *Iterative solution of nonlinear equations in several variables*, volume 30. Siam, 1970.

[173] Steven E Laux. Techniques for small-signal analysis of semiconductor devices. *IEEE Transactions on Electron Devices*, 32(10):2028–2037, 1985.

[174] M Sakhaf and M Schmeits. Capacitance and conductance of semiconductor heterojunctions with continuous energy distribution of interface states. *Journal of applied physics*, 80(12):6839–6848, 1996.

[175] M. Schmeits, N. D. Nguyen, and M. Germain. Competition between deep impurity and dopant behavior of Mg in GaN Schottky diodes. *J. Appl. Phys.*, 89(3):1890–1897, 2001.

[176] N D Nguyen and M Schmeits. Numerical simulation of impedance and admittance of OLEDs. *Phys. Status Solidi (a)*, 203(8):1901–1914, 2006.

[177] B. Vincent, Y. Shimura, S. Takeuchi, T. Nishimura, G. Eneman, A. Firrincieli, J. Demeulemeester, A. Vantomme, T. Clarysse, O. Nakatsuka, S. Zaima, J. Dekoster, M. Caymax, and R. Loo. Characterization of GeSn materials for future Ge pMOSFETs source/drain stressors. *Microelectronic Engineering*, 88(4):342–346, April 2011.

[178] S Wirths, AT Tiedemann, Zoran Ikonic, P Harrison, B Holländer, T Stoica, G Mussler, Maksym Myronov, JM Hartmann, D Grützmacher, et al. Band engineering and growth of tensile strained Ge/(Si) GeSn heterostructures for tunnel field effect transistors. *Applied physics letters*, 102(19):192103, 2013.

[179] Genquan Han, Shaojian Su, Qian Zhou, Pengfei Guo, Yue Yang, Chunlei Zhan, Lanxiang Wang, Wei Wang, Qiming Wang, Chunlai Xue, et al. Dopant segregation and nickel stanogermanide contact formation on source/drain. *Electron Device Letters, IEEE*, 33(5):634–636, 2012.

[180] Roger Loo, Benjamin Vincent, Federica Gencarelli, Clement Merckling, Arul Kumar, Geert Eneman, Liesbeth Witters, Wilfried Vandervorst, Matty Caymax, Marc Heyns, et al. Ge1-xSnx materials: Challenges and applications. *ECS Journal of Solid State Science and Technology*, 2(1):N35–N40, 2013.

[181] Suyog Gupta, Robert Chen, Benjamin Vincent, Dennis Lin, Blanka Magyari-Kope, Matty Caymax, Johan Dekoster, James S Harris, Yoshio Nishi, and Krishna C Saraswat. (Invited) GeSn Channel n and p MOSFETs. *ECS Transactions*, 50(9):937–941, 2013.

[182] Xiao Gong, Genquan Han, Fan Bai, Shaojian Su, Pengfei Guo, Yue Yang, Ran Cheng, Dongliang Zhang, Guangze Zhang, Chunlai Xue, Buwen Cheng, Jisheng Pan, Zheng Zhang, Eng Soon Tok, Dimitri Antoniadis, and Yee-Chia Yeo. Germanium-Tin (GeSn) p-Channel MOSFETs Fabricated on (100) and (111) Surface Orientations With Sub-400C Si2H6 Passivation. *IEEE Electron Device Letters*, 34(3):339–341, March 2013.

[183] Osamu Nakatsuka, Norimasa Tsutsui, Yosuke Shimura, Shotaro Takeuchi, Akira Sakai, and Shigeaki Zaima. Mobility Behavior of Ge $_{1-x}$ Sn $_{x}$ Layers Grown on Silicon-on-Insulator Substrates. *Japanese Journal of Applied Physics*, 49(4):04DA10, April 2010.

[184] Tsuyoshi Nishimura, Osamu Nakatsuka, Yosuke Shimura, Shotaro Takeuchi, Benjamin Vincent, Andre Vantomme, Johan Dekoster, Matty Caymax, Roger Loo, and Shigeaki Zaima. Formation of Ni (Ge 1- xSnx) layers with solid-phase reaction in Ni/Ge 1- xSnx/Ge systems. *Solid-State Electronics*, 60(1):46–52, 2011.

[185] A Dimoulas, P Tsipas, A Sotiropoulos, and EK Evangelou. Fermi-level pinning and charge neutrality level in germanium. *Applied physics letters*, 89(25):252110–252110, 2006.

[186] Y. Shimura, S. Takeuchi, O. Nakatsuka, B. Vincent, F. Gencarelli, T. Clarysse, W. Vandervorst, M. Caymax, R. Loo, A. Jensen, D.H. Petersen, and S. Zaima. In-situ Ga doping of fully strained Ge1-xSnx heteroepitaxial layers grown on Ge(001) substrates. *Thin Solid Films*, 520(8):3206–3210, February 2012.

[187] T Clarysse, P Eyben, B Parmentier, B Van Daele, A Satta, W Vandervorst, Rong Lin, Dirch Hjorth Petersen, and Peter Folmer Nielsen. Advanced carrier depth profiling on Si and Ge with M4PP. In *AVS INSIGHT-2007 Workshop*, 2007.

[188] Vijay R. D'Costa, John Tolle, Junqi Xie, José Menéndez, John Kouvetakis, Marília Caldas, and Nelson Studart. Transport properties of doped GeSn alloys. pages 57–58, 2010.

[189] Federica Gencarelli, Benjamin Vincent, Jelle Demeulemeester, Andre Vantomme, Alain Moussa, Alexis Franquet, Arul Kumar, Hugo Bender, Johan Meersschaut, Wilfried Vandervorst, and others. Crystalline properties and strain relaxation mechanism of CVD grown GeSn. *ECS Journal of Solid State Science and Technology*, 2(4):P134–P137, 2013.

[190] Amporn Poyai, Eddy Simoen, Corneel Claeys, A Czerwinski, and Eugenijus Gaubas. Improved extraction of the activation energy of the leakage current in silicon p–n junction diodes. *Applied Physics Letters*, 78(14):1997–1999, 2001.

[191] A Czerwinski, Eddy Simoen, Amporn Poyai, and Corneel Claeys. Activation energy analysis as a tool for extraction and investigation of p–n junction leakage current components. *Journal of applied physics*, 94(2):1218–1221, 2003.

[192] Roland Scheer. Activation energy of heterojunction diode currents in the limit of interface recombination. *Journal of Applied Physics*, 105(10):4505, 2009.

[193] VP Markevich, AR Peaker, B Hamilton, VV Litvinov, Yu M Pokotilo, SB Lastovskii, J Coutinho, A Carvalho, MJ Rayson, and PR Briddon. Tin-vacancy complex in germanium. *Journal of Applied Physics*, 109(8):083705, 2011.

[194] MB Gonzalez, Eddy Simoen, Geert Eneman, Brice De Jaeger, G Wang, Roger Loo, and Cor Claeys. Defect assessment and leakage control in Ge junctions. *Microelectronic Engineering*, 125:33–37, 2014.

[195] O Breitenstein, J Bauer, A Lotnyk, and J-M Wagner. Defect induced non-ideal dark I–V characteristics of solar cells. *Superlattices and Microstructures*, 45(4):182–189, 2009.

[196] Mei Zhao, Renrong Liang, Jing Wang, and Jun Xu. Improved electrical properties of Ge metal-oxide-semiconductor devices with HfO2 gate dielectrics using an ultrathin GeSnOx film as the surface passivation layer. *Applied Physics Letters*, 102(14):142906, 2013.

[197] Florence Bellenger, Michel Houssa, Annelies Delabie, Thierry Conard, Matty Caymax, Marc Meuris, Kristin De Meyer, and Marc Heyns. Electrical Passivation of the (100) Ge Surface by Its Thermal Oxide. *ECS Transactions*, 11(4):451–459, 2007.

[198] David P Brunco, Brice De Jaeger, Geert Eneman, Alessandra Satta, Valentina Terzieva, Laurent Souriau, Frederik E Leys, Geoffrey Pourtois, Michel Houssa, Karl Opsomer, et al. Germanium: The past and possibly a future material for microelectronics. *ECS Transactions*, 11(4):479–493, 2007.

[199] Suyog Gupta, Robert Chen, James S Harris, and Krishna C Saraswat. Atomic layer deposition of Al2O3 on germanium-tin (GeSn) and impact of wet chemical surface pre-treatment. *Applied Physics Letters*, 103(24):241601, 2013.

[200] Somya Gupta, Benjamin Vincent, B Yang, Dennis Lin, Federica Gencarelli, J-YJ Lin, R Chen, Olivier Richard, Hugo Bender, B Magyari-Köpe, et al. Towards high mobility GeSn channel nMOSFETs: Improved surface passivation using novel ozone oxidation method. In *Electron Devices Meeting (IEDM), 2012 IEEE International*, pages 16–2. IEEE, 2012.

[201] D Buca, S Winnerl, St Lenk, S Mantl, and Ch Buchal. Metal–germanium–metal ultrafast infrared detectors. *Journal of applied physics*, 92(12):7599–7605, 2002.

[202] J Werner, M Oehme, M Schmid, M Kaschel, A Schirmer, E Kasper, and J Schulze. Germanium-tin pin photodetectors integrated on silicon grown by molecular beam epitaxy. *Applied Physics Letters*, 98(6):061108, 2011.

[203] Tso-Ping Ma and Paul V Dressendorfer. *Ionizing radiation effects in MOS devices and circuits*. John Wiley & Sons, 1989.

[204] Stephan Wirths, Daniela Stange, Maria-Angela Pampillón, Andreas T Tiedemann, Gregor Mussler, Alfred Fox, Uwe Breuer, Bruno Baert, Enrique San Andrés, Ngoc D Nguyen, et al. High-k gate stacks on low bandgap tensile strained Ge and GeSn alloys for field-effect transistors. *ACS applied materials & interfaces*, 7(1):62–67, 2014.

[205] JR Brews. A simplified high-frequency MOS capacitance formula. *Solid-State Electronics*, 20(7):607–608, 1977.

[206] C Merckling, X Sun, Y Shimura, A Franquet, B Vincent, S Takeuchi, W Vandervorst, O Nakatsuka, S Zaima, R Loo, et al. Molecular beam deposition of Al 2 O 3 on p-Ge (001)/Ge 0.95 Sn 0.05 heterostructure and impact of a Ge-cap interfacial layer. *Applied Physics Letters*, 98(19):192110–192110, 2011.

[207] Ching-Wei Lee, Yung-Hsien Wu, Ching-Heng Hsieh, and Chia-Chun Lin. Epitaxial GeSn film formed by solid phase epitaxy and its application to Yb2O3-gated GeSn metal-oxide-semiconductor capacitors with sub-nm equivalent oxide thickness. *Applied Physics Letters*, 105(20):203508, 2014.

[208] HG Grimmeiss and C Ovrén. Fundamentals of junction measurements in the study of deep energy levels in semiconductors. *Journal of Physics E: Scientific Instruments*, 14(9):1032, 1981.

[209] M Germain, M El Yacoubi, R Evrard, W Taudt, and M Heuken. Measurements of transient photocapacitance and photocurrent on MOVPE-grown Au/ZnSe/GaAs heterostructures. *Journal of crystal growth*, 184:199–202, 1998.

[210] A Armstrong, G Thaler, and DD Koleske. Deep level investigation of p-type GaN using a simple photocurrent technique. *Journal of Applied Physics*, 105(4):3712, 2009.

Publications and communications

Journal papers

- **Baert, B.**, Gupta, S., Gencarelli, F., Loo, R., Simoen, E., & Nguyen, N. D. (2015). Electrical characterization of p-GeSn/n-Ge diodes with interface traps under dc and ac regimes. *Solid-State Electronics*, **110**, 65-70. http://hdl.handle.net/2268/178856

- Wirths, S., Stange, D., Pampillon, M.-A., Tiedemann, A., Mussler, G., Fox, A., Breuer, U., **Baert, B.**, San Andres, E., Nguyen, N. D., Hartmann, J.-M., Ikonic, Z., Mantl, S., & Buca, D. (2015). High-k Gate Stacks on Low Bandgap Tensile Strained Ge and GeSn Alloys for Field-Effect Transistors. *ACS Applied Materials and Interfaces*, 7, 62-67. http://hdl.handle.net/2268/196534

- **Baert, B.**, Schmeits, M., & Nguyen, N. D. (2014). Study of the energy distribution of the interface trap density in a GeSn MOS structure by numerical simulation of the electrical characteristics. *Applied Surface Science*, **291**, 25-30.
http://hdl.handle.net/2268/156365

- **Baert, B.**, Nakatsuka, O., Zaima, S., & Nguyen, N. D. (2013). Impedance Spectroscopy of GeSn-based Heterostructures. *ECS Transactions*, **50**(9), 481-490. http://hdl.handle.net/2268/127051

Oral communications and posters

- **Baert, B.**, Gupta, S., Gencarelli, F., Loo, R., Simoen, E., & Nguyen, N. D. (2015, September). *Analysis of the time-dependent electrical current in reverse-biased p-GeSn/n-Ge mesa diodes.* Poster session

presented at E-MRS 2015 Fall Meeting.
http://hdl.handle.net/2268/187525

- **Baert, B.**, Gupta, S., Gencarelli, F., Shimura, Y., Loo, R., Simoen, E., & Nguyen, N. D. (2015). *Reverse current transient behavior of pGeSn/nGe diodes.* Paper presented at The 9th International Conference on Silicon Epitaxy and Heterostructures (ICSI 9), Montréal, Canada. http://hdl.handle.net/2268/178857

- **Baert, B.**, Cerica, D., Schmeits, M., & Nguyen, N. D. (2014, November 13). *Electrical modelling of interface traps in GeSn MOS structures.* Paper presented at JSPS International Core-to-Core Program Workshop on Atomically Controlled Processing for Ultra-large Scale Integration, Leuven, Belgium. http://hdl.handle.net/2268/174386

- **Baert, B.**, Gupta, S., Gencarelli, F., Loo, R., Simoen, E., & Nguyen, N. D. (2014, September 15). *Impact of traps on the electrical characteristics of GeSn/Ge diodes.* Poster session presented at E-MRS 2014 Fall Meeting - Symposium J, Warsaw, Poland.
http://hdl.handle.net/2268/174383

- **Baert, B.**, Gupta, S., Gencarelli, F., Loo, R., Simoen, E., & Nguyen, N. D. (2014, June 03). *Electrical characterization of pGeSn/nGe diodes.* Paper presented at 7th International Silicon-Germanium Technology and Device Meeting (2014 ISTDM), Singapore.
http://hdl.handle.net/2268/169299

- Gupta, S., Simoen, E., Asano, T., Nakatsuka, O., Gencarelli, F., Shimura, Y., Moussa, A., Loo, R., Zaima, S., **Baert, B.**, Dobri, A., Nguyen, N. D., & Heyns, M. (2013, June 04). *Electrical Activity of Threading Dislocations and Defect Complexes in GeSn Epitaxial Layers.* Paper presented at The 8th International Conference on Silicon Epitaxy and Heterostructures (ICSI-8), Fukuoka, Japon.
http://hdl.handle.net/2268/146619

- **Baert, B.**, Gupta, S., Schmeits, M., Simoen, E., & Nguyen, N. D. (2013, June). *Study of interface trap density in a GeSn MOS structure by numerical simulation of the electrical characteristics.* Poster session presented at The 8th International Conference on Silicon Epitaxy and Heterostructures (ICSI-8), Fukuoka, Japan.
http://hdl.handle.net/2268/146470

- **Baert, B.**, Schmeits, M., & Nguyen, N. D. (2013, May). *Study of interface trap density in a GeSn MOS structure by numerical simulation of the electrical characteristics.* Paper presented at European Materials Research Society (E-MRS) 2013 Spring Meeting. http://hdl.handle.net/2268/144526

- **Baert, B.**, & Nguyen, N. D. (2012, June). Numerical Simulation of the Electrical Characteristics of GeSn/Ge Semiconducting Heterostructures. Poster session presented at "Jaszowiec" International School and Conference on the Physics of Semiconductors. http://hdl.handle.net/2268/117951

- **Baert, B.**, Nakatsuka, O., Zaima, S., & Nguyen, N. D. (2012). Impedance spectroscopy of GeSn/Ge heterostructures by a numerical method. *222nd ECS Meeting, 2012.* ECS. http://hdl.handle.net/2268/126180

- **Baert, B.**, Truong, D. Y. N., Nakatsuka, O., Zaima, S., & Nguyen, N. D. (2012). *Electrical Characterization of p-Ge1-xSnx/p-Ge and p-Ge1-xSnx/n-Ge Heterostructures by Numerical Simulation of Admittance Spectroscopy.* Poster session presented at 6th International SiGe Technology and Device Meeting (ISTDM), Berkeley, CA. http://hdl.handle.net/2268/115788