Resistivity percolation of co-sputtered amorphous Si/Ti films

G. Lewis [a], Z. Moktadir [a], M. Kraft [a], Liudi Jiang [b],*

[a] School of Electronics and Computer Science, University of Southampton, Southampton SO17 1BJ, United Kingdom
[b] School of Engineering Sciences, University of Southampton, Southampton SO17 1BJ, United Kingdom

ARTICLE INFO

ABSTRACT

Amorphous silicon/titanium (a-Si/Ti) composite was deposited by co-sputtering techniques at room temperature with a view to explore its potential applications for monolithic integration of micro-electro-mechanical systems (MEMS) and integrated circuits. The electrical resistivity of the films was successfully controlled over a range of magnitudes and the electrical transport mechanism was studied, based on percolation conduction theory of a three dimensional random network. The stability of the nanostructures and thus the percolation threshold was also observed at annealing temperatures below 300 °C, while the percolation threshold decreased with annealing temperature above 300 °C. Surface morphology and dry etching feasibility of the composite are also discussed for the potential applications of using it as the structural device layer for MEMS.

1. Introduction

The monolithic integration of micro-electro-mechanical systems (MEMS) sensors and actuators directly on top of their driving and signal processing electronic circuitries has attracted considerable interest as it enables tighter integration of MEMS and associated integrated circuits (IC), leading to cost-effective systems with high performance. However, the technical realisation of this integration has been hindered mainly by high temperature (>600 °C) deposition required by polycrystalline silicon (poly-Si) [1], which is commonly used as structural material for MEMS. Recently, a-Si has been developed [2–4] as a promising alternative because it can be deposited at low temperatures (<250 °C). Most of the mechanical properties of a-Si are similar to those of poly-Si [4]. A-Si can also be easily integrated with low-cost Si-based IC and MEMS fabrication processes. Nevertheless, a-Si is usually dielectric and difficult to dope effectively. Thus it is unsuitable for many MEMS applications such as electrostatic and eletrothermal devices. Metal layers had to be employed as conductive claddings for a-Si MEMS [5], which complicates the microfabrication process and introduces parasitic stress potentially causing deterioration of device performance.

In this work, co-sputtered a-Si/Ti nanocomposites have been deposited at low temperatures as a novel structural material, which is potentially suitable for above-IC MEMS. As a focus of this study, the electrical property of the a-Si matrix was tailored through the incorporation of Ti nanoparticulates. Ti was chosen because it can be effectively dry etched using the fluorinated and chlorinated chem-istries [6], commonly used for Si surface micromachining. The electrical percolation conduction mechanism of the composite films was systematically investigated. It was found that the resistivity of a-Si/Ti exhibits a power law dependence on the Ti content with an exponent β equals to 2. Characterisation of surface morphology and dry etching of a-Si/Ti films was also carried out and discussed for their potential MEMS applications.

2. Experimental

Si chips (10 mm×10 mm) covered with thermal oxide (SiO$_2$) of 1 μm thickness were used as deposition substrates. A multi-substrate holder was employed to cover all edges of the substrates during deposition, preventing contacts between deposited layers and the Si substrates on the sides. Co-sputtering of high purity Si (99.999%) and Ti (99.95%) targets was carried out using DC and RF power supplies, respectively, in a Kurt J. Lester sputterer. By adjusting the power of the Ti target while keeping the power of the Si target constant, the percentage of Ti in the deposited films was controlled. Argon was used as sputtering gas and the chamber pressure was kept at 8×10^{-3} mbar. Substrates were maintained at room temperature for all depositions. For each deposition, a-Si/Ti film on an Al substrate was also produced, which was subsequently used for material characterisation using the Energy Dispersive X-ray (EDX) analysis method. The motivation to use Al substrates was to eliminate possible Si spectra from the SiO$_2$/Si substrates and thus ensure all Si EDX spectra can be attributed to the deposited layers. The relative Ti and Si weight percentages of the composite films were determined by subtracting the background Al and oxygen spectra. A selection of co-sputtered samples was subsequently annealed at temperatures (T_A) from 200 to 500 °C for 2 h in ambient atmosphere to investigate the stability of the electrical

properties and nanostructures of a-Si/Ti. The sheet resistance of the films was measured using four-point probe method. The thickness of the deposited films ranges from 190 nm to 390 nm which was measured using a KLA Tencor stylus profiler. The electrical resistivity of the films was calculated using the measured values of sheet resistance and thickness. Nanostructure and surface morphology of the films were examined using an Atomic Force Microscope (AFM) (Asylum Research MFP-3D). Preliminary dry etching trials of the deposited composite films were conducted in a reactive ion etch (RIE) reactor using SF_6 (20 sccm) and O_2 (10 sccm) gas mixture.

3. Results and discussion

Typical RMS roughness is around 0.6–1.5 nm for deposited films with thickness of approximately 290 nm–390 nm and a typical AFM section profile is shown in Fig. 1. It is anticipated that the surface roughness could be further improved by lowering the sputtering pressure to meet the requirement (roughness<0.5 nm) [7] for wafer bonding processes as an important microfabrication procedure for MEMS. As such a-Si/Ti could also be employed for micro-opto-electro-mechanical systems (MOEMS) applications. The granular structures of the as-deposited and annealed samples are clearly shown in Fig. 2. The average grain size increases with annealing temperatures from approximately 20 nm at room temperature to approximately 40 nm at 500 °C. Nevertheless, compared with that of the as-deposited films, the annealing process did not cause an obvious increase of surface roughness.

As a primary aim of this work, the electrical resistivity of the a-Si/Ti films was systematically studied. Fig. 3 shows that the resistivity of the a-Si/Ti films can be tailored over a wide range as a function of the Ti percentage at different annealing temperatures. It was observed that the dependence of the resistivity on the Ti content in the composite films is in excellent agreement with the percolation theory [8] as the resistivity scales as

$$\rho = a(T)(X - X_c(T))^{-\beta} \qquad (1)$$

where $a(T)$ is temperature dependant prefactor, X is the Ti percentage and β is the critical exponent. $X_c(T)$ is the percolation threshold, i.e. the Ti percentage, at which a continuous transport network is formed by the metallic grains and thus metallic transition occurs [9]. $X_c(T)$ depends on the system dimension and symmetry, while the critical exponent β depends on system dimension only. $X_c(T)$ and $a(T)$ were derived by fitting Eq.(1) to the experimental data using nonlinear regression as shown in Fig. 4. Since a critical exponent $\beta \approx 2$ is typical in many granular films (such as co-sputtered Au-SiO$_2$ [10]), in this study, β was initially set to 2 to obtain the best fit (Fig. 3), which was determined by the R-square test for the parameters $a(T)$ and $X_c(T)$. The R-square value for this fits was 99% for all values except for $T_A = 500$ °C where the R-square value was 96%. To confirm this scaling behaviour, X/X_c versus $\rho X_c^\beta / a$ was plotted in Fig. 5, which shows a good data collapses into single curve of $y = (x - 1)^{-2}$. This data collapse justifies the value of $\beta = 2$ and suggests that all the investigated a-Si/Ti films are three dimensional (3D), where the grain sizes are much smaller than the thickness of the films [11].

The a-Si/Ti films can be viewed as a random resistor network where grains are either conductive for Ti or non-conductive for Si. Indeed, the universality of β was confirmed by several numerical computations of random resistor network models where $\beta \approx 2$ for 3D lattices [12,13]. A similar study of co-sputtered silicon–titanium deposited on poly-Si and SiO_2 substrates was reported by Murarka and Fraser [14]. They found evidence of a titanium silicide ($TiSi_2$) component after annealing of the films in temperature ranging from 600 °C to 1000 °C. No alloyed $TiSi_2$ were found below 500 °C. More importantly, the presence of $TiSi_2$ induced a decrease of the film resistivity, which is in contrast to our observations where the resistivity increased with annealing temperatures (Fig. 3) up to
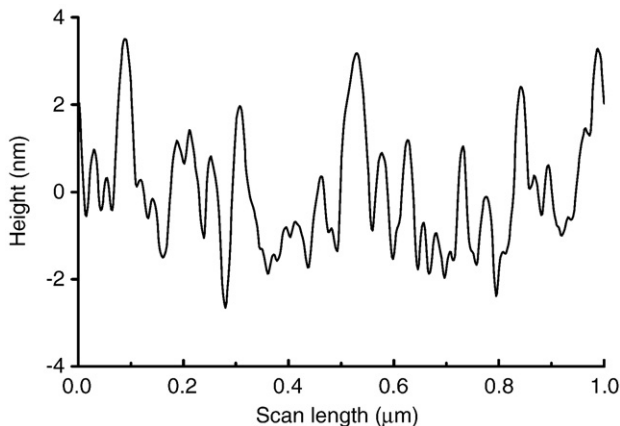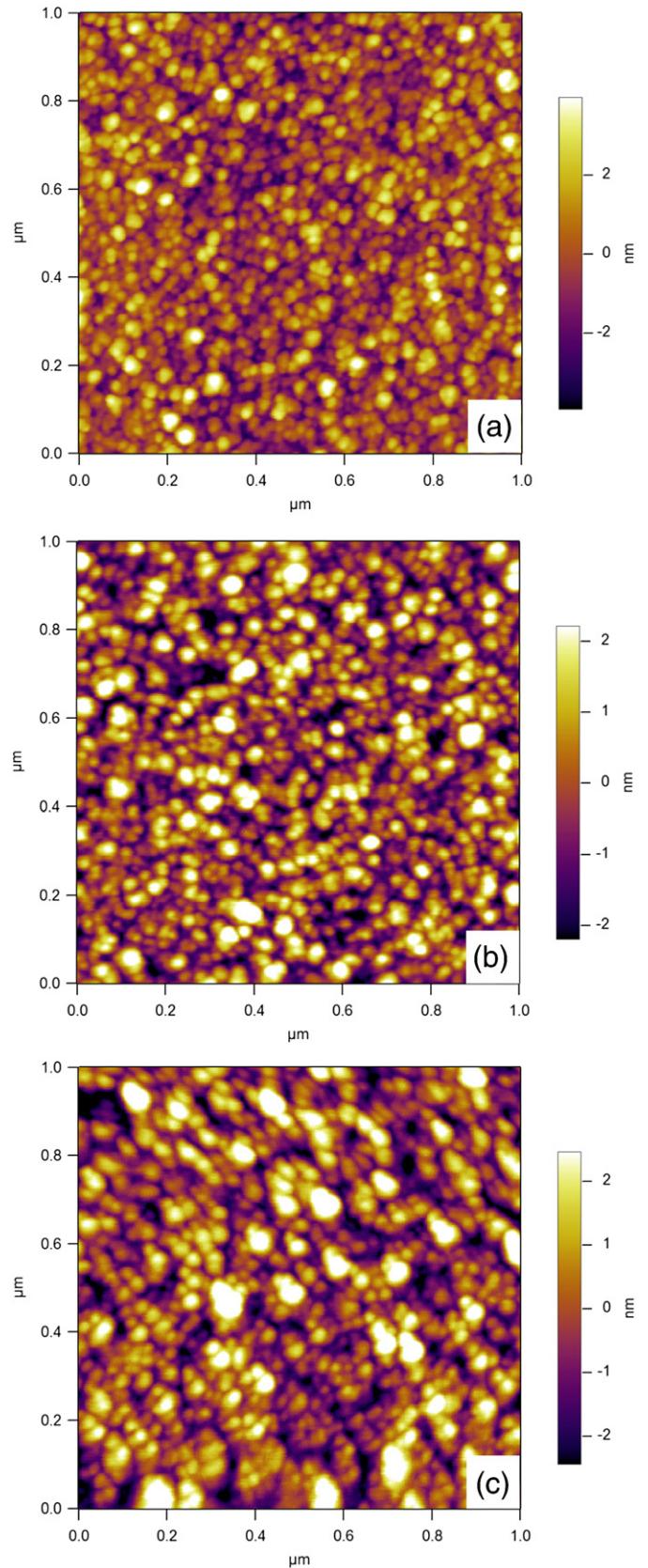

Fig. 2. AFM images of (a) un-annealed, (b) 300 °C annealed, (c) 500 °C annealed a-Si/Ti films. (For interpretation of the references to colour in this figure legend, the reader is referred to the web version of this article.)

500 °C. These observations alongside the percolation behaviour is a strong evidence that there are no silicide present in our composite films and that these films can be viewed as a 3D random network of Ti and Si grains. The constant value of β indicates that the grain size

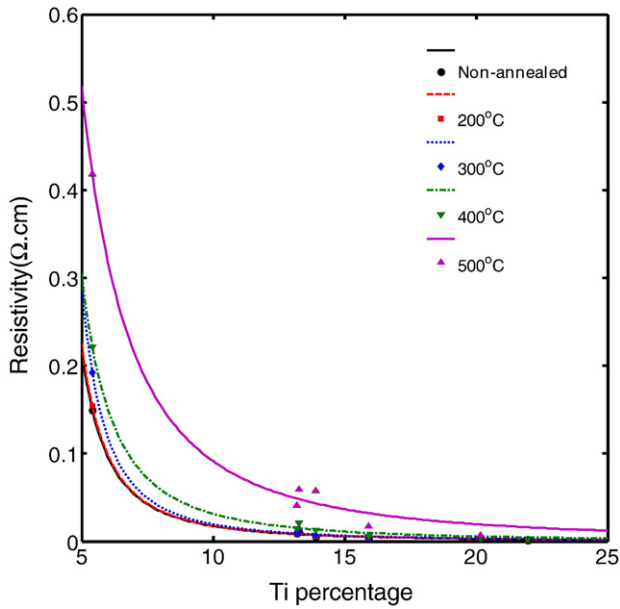**Fig. 1.** AFM section analysis of a deposited a-Si/Ti film.

Fig. 3. Resistivity of a-Si/Ti as a function of Ti percentage. The solid lines are the regression fits to Eq. (1). (For interpretation of the references to colour in this figure legend, the reader is referred to the web version of this article.)

Fig. 5. Data collapse in X/X_c versus $\rho X_c^{\beta}/a$ at different annealing temperatures ($\beta=2$). (For interpretation of the references to colour in this figure legend, the reader is referred to the web version of this article.)

remained small in all experimental conditions, compared to the films thickness. Thus the dimensionality of the problem remains unchanged for annealing processes with $T_A \le 500$ °C. On the other hand, Fig. 4 shows that X_c decreases and $a(T)$ increases when $T_A > 300$ °C. These two parameters are determined by the composite nanostructures and the mean inter-grain junction conductance. During annealing the grains undergo coalescence and as a consequence their average size increases as evidenced in Fig. 2. X_c is the minimum fraction of Ti, for which at least one group of grains expands from one side to the opposite one of the area in consideration (a percolation path). We attribute the decrease of X_c to the coarsening of grains at $T_A > 300$ °C, which induces the formation of percolation paths. Furthermore, constant X_c for $T_A \le 300$ °C (typically ~3% in Fig. 4) indicates the electrical stability of the nanostructured a-Si/Ti composite films for this temperature range sufficient for above-IC MEMS applications.

Dry etching is a key patterning technique for the MEMS fabrication. The feasibility of a-Si/Ti subject to dry etching was preliminary studied in this work by carrying out RIE on the deposited a-Si and a-Si/Ti films, using an unoptimised etching recipe. Effective dry etching of a-Si/Ti was observed and the etch rate changes with the Ti percentage (e.g.
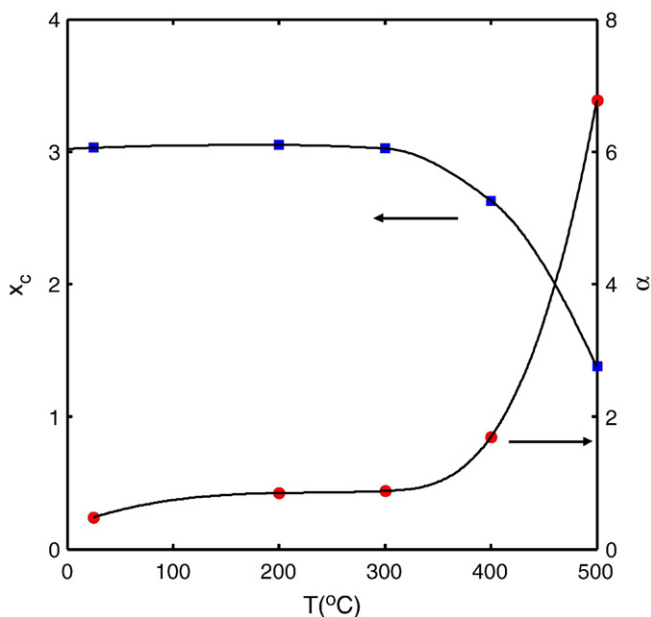
104 nm/min for a-Si and 71 nm/min for a-Si/5.4%Ti). Optimisation of etching processes is required to maximize etch rates for a-Si/Ti, which is being addressed in future work.

4. Conclusions

Co-sputtering technique was used to deposited a-Si/Ti film at low temperatures in order to investigate its suitability for above-IC MEMS applications. The electrical properties of the deposited films were effectively tailored as a function of the Ti percentage. A percolation study suggests a 3D composite system for both the as-deposited and annealed a-Si/Ti films. The study of the percolation threshold on annealed samples indicates the nanostructure stability of a-Si/Ti with $T_A \le 300$ °C. This study provided us with an understanding of the electrical properties of this material and allowed us an insight into the physical mechanism behind those properties, which are important for potential low temperature MEMS processes. Furthermore, the a-Si/Ti films possess smooth surfaces and can be patterned using commonly available dry etching techniques. The combination of these material and process advantages suggests that a-Si/Ti has the potential to be a compelling structural material for future above-IC MEMS.

Fig. 4. X_c and α as a function of the annealing temperature. (For interpretation of the references to colour in this figure legend, the reader is referred to the web version of this article.)
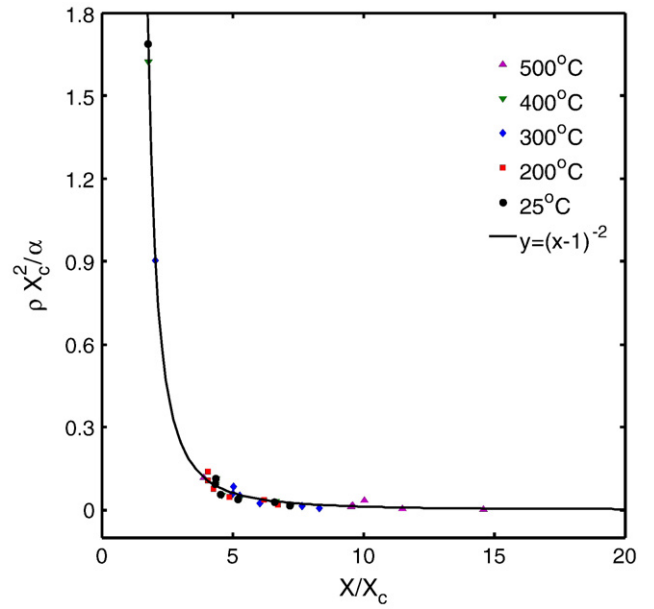
References

[1] French PJ, van Drieenhuizen BP, Poenar D, Goosen JFL, Mallee R, Sarro PM, et al. J Microelectromech Syst 1996;5:187–96.
[2] Pal P, Chandra S. J Micromech Microeng 2005;15:1536–46.
[3] Chung CK, Tsai MQ, Tsai PH, Lee C. J Micromech Microeng 2005;15:136–42.
[4] Chang S, Sivoththaman S. J Micromech Microeng 2006;16:1307–13.
[5] Honer KA, Kovacs GTA. Sens Actuators A 2001;91:386–97.
[6] Parker ER, Thibeault BJ, Aimi MF, Rao MP, MacDonald NC. J Electrochem Soc 2005;152:C675–83.
[7] Schmidt MA. Proc of Solid-State Sensor and Actuator Workshop at Hilton Head; 1994. p. 127–31.
[8] Dorfman BF. Thin Solid Films 1998;330:76–82.
[9] Abeles B, Pinch HL, Gittleman JI. Phys Rev Lett 1975;35:247–50.
[10] McAlister SP, Inglis AD, Kayll PM. Phys Rev B 1985;31:5113–20.
[11] Takayama T, Odagaki T. J of the Phys Soc of Japan 2001;70:3176–7.
[12] Clerc JP, Podolskiy VA, Sarychev K. Eur Phys J B 2000;15:507–16.
[13] Batrouni GG, Hansen A, Larson B. Phys Rev E 1996;53:2292–7.
[14] Murarka SP, Fraser DB. J Appl Phys 1980;51:350–6.